Part #0115-0100

1 March 1978

A46752

MODEL 1015

WAVEFORM RECORDER

OPERATING AND SERVICE MANUAL

biomation

4600 old ironsides drive, santa clara, ca. 95050 • (408) 988-6800 • TWX (910) 338-0509

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INSTRUMENT SHOP

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SECTION I

General Information

1.1 Certification

Biomation Corporation certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages. See back of manual for full warranty statement.

1.3 Instrument Description

The Biomation Model 1015 Waveform Recorder provides performance and features not previously available in a multi-channel portable recorder. Up to four simultaneous analog input signals with bandwidths to 25 kHz can be recorded. The recorded resolution of each input signal is one part in 1024 (better than 1/10 per cent).

Numerous selectable record rates are provided along with versatile control and triggering functions with a digitally adjustable delay of as much as 10 times the record length. One of these trigger delay and control functions permit the trigger to be received before, during, or after the signal has occurred. This unique "pretrigger" capability ensures capture of the leading baseline and rise of a random signal.

Easy-to-use front-panel selector switches permit the unit to be configured as a single channel recorder with four times the recording time - while retaining an input bandwidth of up to 25 kHz. Or as a two-channel unit with twice the record time per channel. The unit may also be set to record up to four separate signals, one-at-a-time, from a single input into each

of the four storage channels while "holding" each previously recorded signal.

The output features of the unit are as convenient and useful as the input and record functions. Three types of outputs are provided. The digital output produces 10-bit amplitude data with bit parallel/word serial interface at standard TTL levels. Analog outputs are provided in two forms. A repetitive analog output is produced which provides a flicker-free display on an oscilloscope or CRT display. A very slow analog output is available to reproduce the recorded signals on a strip-chart or X-Y recorder.

In addition, a versatile feature is included which permits the user to display on a CRT or plot on an X-Y recorder the signal from one channel versus the signal on another channel. This X versus Y output feature gives the ability to immediately examine the relationships between variables for signals with bandwidths from dc to very high audio frequencies.

Another feature which extends the usefulness of the 1015 is the provision of inputs and outputs of the record clock rate and triggering signals for conveniently synchronizing the operation of several units. Thus 8, 12 or more channels can be readily implemented.

The Model 1015 is a bench-type instrument with tilt-up stand and may also be rack mounted, occupying a 7-inch vertical space in a standard 19" wide rack.

Specifications for the Model 1015 are given in the following paragraphs.

1.4 Performance Specifications

Input Channels. Four independent channels.

Input Impedance. One megohm each input to ground with 50 pf parallel capacitance.

Input Voltage Range. 100 mV to 50 V full scale each input selectable by 9 position (1–2–5 sequence) switches.

Input Coupling. AC or DC selectable for each input.

Input Offset. Adjustable from zero to ± full scale, each input.

Offscale Indicators. Two LED's for each input indicate signals + or – beyond range of input.

Input Bandwidth. DC to 25 kHz (Optional to 50 kHz) for each input. Low frequency 3 db cutoff at 1.6 Hz on AC coupling.

A/D Converters. Four 10 bit (1 part in 1024) converters.

Sample Rates. Internal: Single or dual rates independently selectable from 0.01 Hz to 10 kHz on 10 position (1–2–5 sequence) switches and msec/sec multiplier switches.
External: Selectable for input of TTL pulses in two pulse rate bands of 5 kHz and slower and from kHz to 100 kHz.

Memory Size: 4096 words x 10 bits/word arranged as four 1024 word memories.

Record Configurations. Front Panel Switch Selectable:

- Single Channel Input w/4096 Word Recording.
- Two Channel Input Into Two 2048 Word Recordings.
- Four Channel Input Into Four 1024 Word Recordings.
- Data In Any 1024 Word Channel(s) Can Be Retained While Recording In Other Channel(s) .
- Single Channel Input Into Any Of The 1024 Word Memories While Retaining Previously Recorded Data In Other Three Memories.

Record Modes. Normal: Recording starts on (delayed) Trigger and stops after one refresh of memory.
Pretrigger: Recording starts on "Arm" and stops on (delayed) Trigger.

Arm Input. Momentary pushbutton or TTL input pulse enables Trigger for single record sweep recording.

Arm Ready. LED indicator lit when Arm enabled.

Trigger Modes. Auto/Normal/Single trigger operation, switch selectable.

Trigger Ready. LED indicator lit when Trigger enabled.

Trigger Detection. Manual: Via pushbutton.
Internal: Any input, switch selectable.
External: Via front panel BNC.
Level: Adjustable 2X full scale (±10 V external), selectable ± slope, AC/DC coupling.

Trigger Delay. Settable via 3 digital switches and proportional to sample rate from 10 samples to 9,990 samples in 10 sample increments.

Data Output. Ten bit parallel TTL levels, pure binary code connected positive or negative true. Asynchronous 'handshake' data exchange with 'Flag' output and 'Command' input control bits. Average rates continuous from 500 x 10^3 words/sec to 10 x 10^3 words/sec. Lower data rates will exhibit up to 1 msec latency. Flag and Command signals TTL levels, positive true. Optionally negative true.

Display Outputs. X, repetitive sweep ramp of 1 volt peak switch selectable to 2, 5, and 10 volts (sweep expand) and switch selectable durations of 1 msec (4-trace display) 2 msec (2-trace display) and 4 msec (1-trace display). Or, selectable as repetitive signal from channel one to produce X vs Y displays with respect to channel 2, 3 and 4 signals. Origin adjustable ±0.5 full scale (position control).
Y, repetitive sequential replica of all recorded signal(s) 0.25 volts full scale, switch expandable to 1.0 volts. Reconstruction rate 1 μsec per word. Each signal selectable Display or Off with individual vertical position controls coordinated with X output selection. Vert positions adjustable ±2X full scale.
Z, 0 to +5 V pulse for CRT blanking or for triggering scopes. Also, output as +5 V to 0 pulse ($\overline{Z}$).

Output Control. Off Plot or Digital outputs not available. Unit reverts to Display Output after recording.
Auto – Single data output (4096 points) available beginning at end of recording. Reverts to Display Output after one complete data output.
Edit - Digital or Plot output enabled upon demand.

Plot Output. Analog replica of each recorded signal output over 100 sec interval (0.1 sec/word). Channels sequentially plotted or individually selectable. ±1 volt full scale amplitude. Concurrent 100 sec, 200 sec or 400 sec ramp produced to provide X plot sweep, 1 V peak. Or 100 sec replicas of signal in channel one to produce X vs Y plots with respect to signals in channels 2, 3 and 4. 0 to +5 volt pen signal also provided, positive during X sweep. Optionally available inverted or as 1 msec pulse.

Multi-Unit Connections. Rear panel connections for synchronous operation of multiple model 1015 units – Time Base Out, Time Base In, Trigger Out, Trigger In.

Size. 6.25" H (16 cm) x 17" W (43 cm) x 19" D (48 cm).

Weight. Approximately 40 pounds (18.2 Kg).

Power. Approximately 100 W, 115/220 V, rms ±10%, 50-60 Hz.

Accessories. Each unit is supplied with a line cord, extender card, and two copies of the Operating and Service Manual.

SECTION II

Installation

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage and installation of the Model 1015.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Santa Clara, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

Line voltage: the Model 1015 may be operated from either 115 or 230 volt (±10%) power lines. The line cord connector contains a line filter.

The desired line voltage may be selected as follows: disconnect the line cord at the instrument. Using a narrow blade screwdriver, slide the voltage selection switch so that the proper line voltage appears on the switch.

For 115 V operation, use a 1.5A slow blow fuse. For 230 V operation, use a .75A slow blow unit.

CAUTION: Before plugging instrument in AC power line, be sure line voltage switch is properly positioned.

. Power cable: The Model 1015 is equipped with a detachable 3-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (3-socket connector) to AC line jack at rear of instrument.

b) Connect plug (2-blade with round grounding pin) to 3-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only 2-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

2.5 Preparation for Use

The Model 1015 is not a "self-contained" instrument in that it must be interfaced with other types of instrumentation in order for the data to be visible or analyzed. The following sections of this manual cover operation, setups and interface requirements.

2.6 Initial Warm-up

Although the Model 1015 is a solid state instrument, a brief warm-up period of approximately 10 minutes is required for the input amplifiers and the analog-to-digital converters to reach thermal stabilization. This warm-up period is recommended for both the Model 1015 and its associated output device.

SECTION III

Principles of Operation

3.1 Introduction

The Model 1015 Waveform Recorder offers superior performance and unique features for many recording tasks traditionally accomplished by electro-mechanical recorders. The 1015 is a member of a new class of solid-state electronic instruments which use digital techniques to record analog signals and subsequently present them in either analog or digital forms for analysis, communication or mass storage.

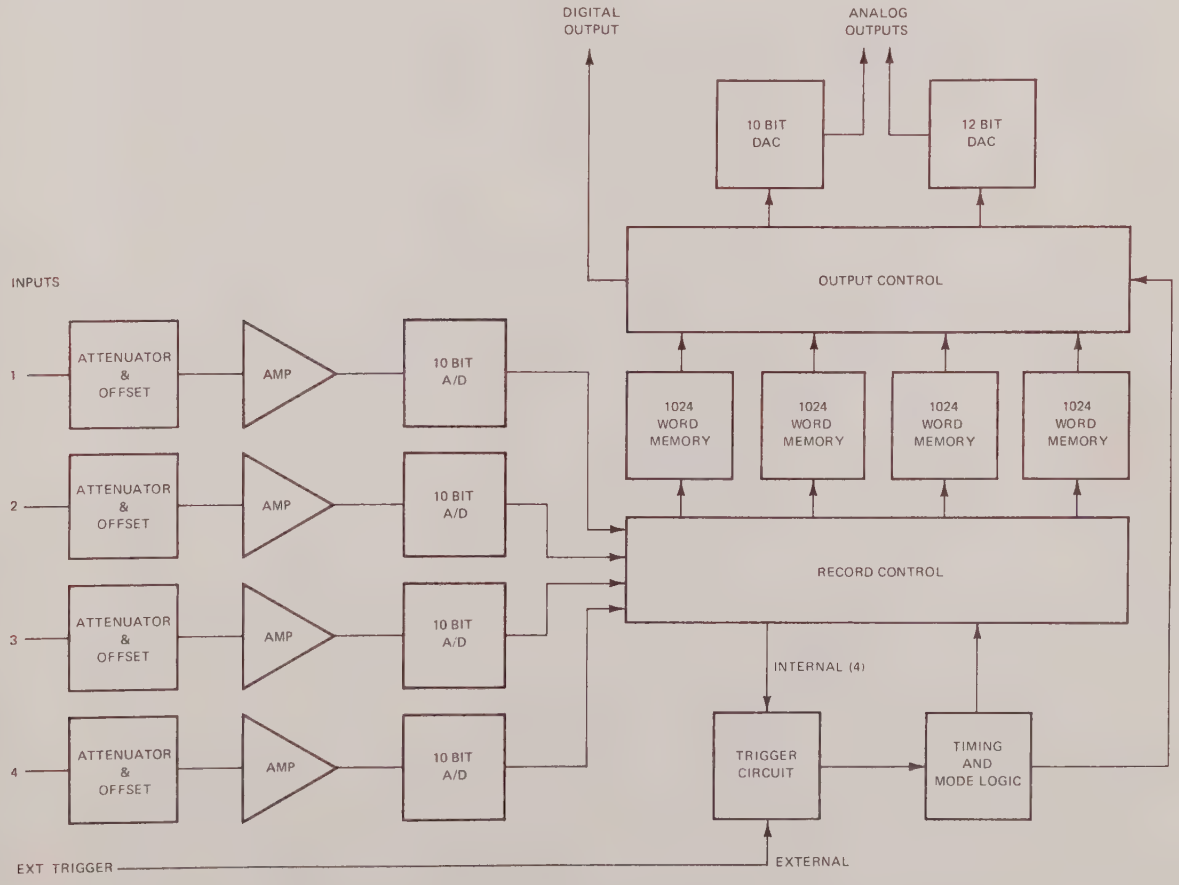


Figure 3.1 Model 1015 Block Diagram

3.2 Basic Functional Description

The waveform recorder as an electronic instrument is conceptually quite simple. Its basic form consists of four A/D converters integrated with four digital memories, all of which are regulated by common timing and control circuitry. Two digital-to-analog converters are also included to produce analog outputs in addition to the digital output. Versatile input offset, triggering, and other user functions are also featured. A simplified block diagram of the Model 1015 is presented in Figure 3.1.

3.21 Signal Inputs

The four input channels each contain an input amplifier with an input attenuator and an input offset control. Independent selection of input sensitivities from 100 mv to 50 volts full scale and offsets on each input signal of up to plus or minus the full scale sensitivity are provided. The impedance of each input is 1 megohm with 50 picofarads parallel capacitance.

Four analog-to-digital converters are utilized, one for each input channel. This permits simultaneous sampling of input signals without the loss of bandwidth which results from the use of an analog multiplexer. The A/D converters are very precise integrating types with full 10-bit resolution and maximum conversion rates of 100 kHz.

3.22 Recording Configurations

The memories in the Model 1015 are MOS shift registers with a total capacity of 4096 x 10-bits arranged as four 1024 word memories. Previously recorded data can be held in each 1024 word memory during subsequent four channel mode recordings by convenient switch selection associated with each input. The input channels and memories are configured to permit the switch selection of single channel recording with 4096 points of storage or two channel recording with 2048 stored points each in addition to the normal four channel/1024 points per channel operation. Also switch selectable is the ability to record from one input into any one of the 1024 word memories while retaining or "holding" the contents of the other memories.

3.23 Trigger and Control Function

The trigger and control circuits include an adjustable delay which is selected via convenient digital switches in increments of ten sample intervals to almost 10,000 sample intervals. This delay along with adjustable level trigger circuits permit the definition of a precise "recording window" with respect to a given or a detected trigger event. The trigger can be detected from the signal on any one of the

input signals or it can be supplied from an external source. In addition, the trigger polarity and coupling are selectable.

A unique capability of the waveform recorder is its ability to record the signal preceding the trigger point. This "pretrigger recording" feature ensures recording of the leading baseline and rise of a signal. This is accomplished by having the unit record continuously until the trigger is received, then using a delayed trigger to stop the recording process, freezing the data in memory that was received in the period preceding the delayed trigger. The trigger delay allows control of the stop point, so the trigger may be near the beginning, middle, or end of the stored information. This also permits the selection of a trigger level well above the noise without losing leading edge information.

3.24 Internal or External Record Rates

Selectable record rates are available from an internal crystal oscillator or an external sample rate input can be used. The nineteen internal sample rates range from 100 kHz to as slow as 0.1 Hz (from 10 µsec to 10 sec per point). The independent selection of two internal record rates is provided which permits dual time base recording when desired. Thus, for example, fast rise/slow decay signals can be recorded with optimum time resolution.

3.25 Digital Output

The digital output from the unit is a bit parallel/word serial data exchange at asynchronous rates of up to 500 K words per second. A data exchange communications signal (one TTL bit) is output (Flag) and a similar input signal is accepted (Command) to effect a convenient and accurate "handshake" data exchange. A 10-bit wide signal data word is produced for each stored data point. The digital signals are all TTL compatible with levels of 0 volt and +4 to +5 volts.

3.26 Analog Outputs

The unit includes two D/A converters which provide analog outputs of the recorded information. Two types of analog outputs are produced. Rapid, repetitive signals are output for presentation on a CRT display and slow analog signals provide hard-copy reproductions of the recorded signals via strip-chart or X-Y plotter.

The CRT display output is a repetitive replica of the recorded signal(s) producing a flicker-free presentation. A four trace presentation on the CRT is produced and

individual vertical position controls are provided for each trace. A linear horizontal sweep ramp is also produced for the CRT and this may be "expanded" up to 10 times to allow full width examination on the CRT of as little as one-tenth of each trace. In addition, each of the four traces can be set to have one-fourth full scale vertical amplitude. Or any of the traces can be viewed individually with full scale vertical amplitude. A single trace of the entire 4096 word memory contents is selectable as well as two CRT traces of 2048 words each.

The two D/A converters can also be set to produce very slow outputs of the signals with a concurrent linear ramp to produce a representation of the signal or signals on an X versus Y recorder. The plot signal output can also, of course, be input to an ordinary strip-chart recorder.

Another analog output mode allows the two D/A converters to be used to simultaneously output from two channels. This gives the ability to present one variable versus another as "X" versus "Y" on a CRT display or on an X-Y plotter. This X versus Y output can be selected to be at the rapid repetitive display rate or the slow plot rate. In either case, the signal in channel one is output via the Normal X output D/A converter and the signals in channels 2, 3 and 4 are output via the "Y" D/A converter producing a Y_1 versus Y_2, Y_3, and/or Y_4 presentation.

3.3 Operational Functions

Recording with the Model 1015 Waveform Recorder resembles in many respects the operation of an oscilloscope. The 1015 does, however, provide greater flexibility, settability and range of control functions than normally found on most oscilloscopes, as well as operational features not possible with an oscilloscope.

The operation of the Model 1015 is basically concerned with the signals or events which determine the initiation and termination of the sampling and recording of the input signals. The basic record control relationships are shown in Figure 3.2 and described in the following subparagraphs.

3.31 Sweep and Sweep Time

In the following discussions the terms "sweep" and "sweep time" are used. The term "sweep" is used to designate the succession of samples taken on the input signals during a recording sequence. The term "sweep time" is used to designate the amount of time required to fill the memories with contiguous samples of the input signals. When this term is used, it is normally assumed that the entire sweep was accomplished at a single linear sample rate.

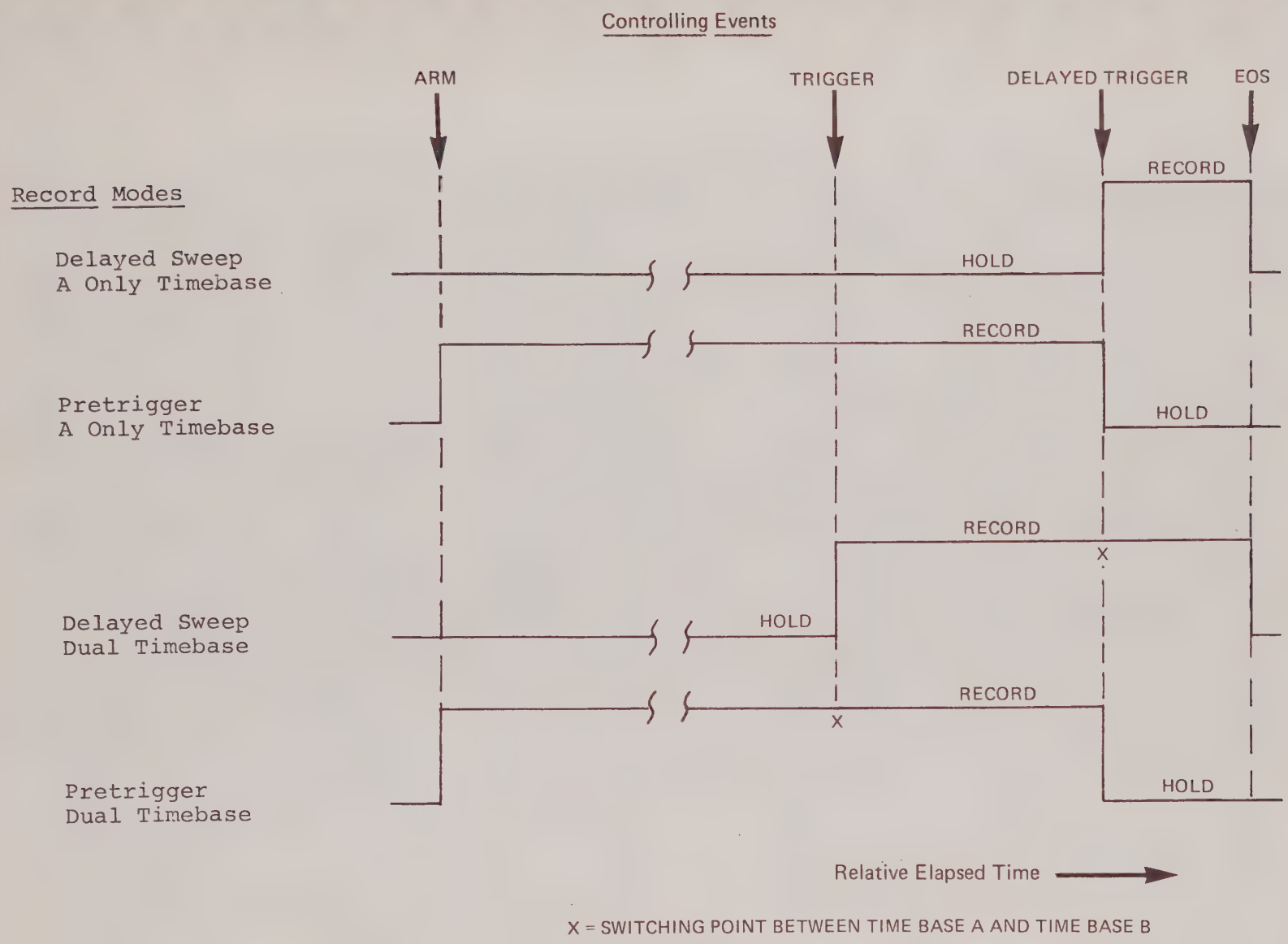


Figure 3.2 Model 1015 Recording Control Functions

3.32 Arm, Trigger and End-of-Sweep Functions

The arm, trigger and end-of-sweep functions, together with an adjustable delay (associated with the trigger event) control the sequence-of-events in the operation of the record cycle of the Model 1015. The effect of each of these functions or events on the sequence-of-events is dependent upon the recording mode selected for the unit.

The arm function could also be termed trigger reset and is required only when the trigger mode is "Single". With the use of Single trigger mode, each record cycle must be initiated by an "Arm" function which allows the unit to accept a trigger function. The arm function can be provided manually via the front panel pushbutton or via a logic level signal into a rear panel connector. The use of the arm feature in Single trigger mode conveniently allows the user to control the recording function of the unit while still ensuring that the actual recorded signals are in a known time relationship with a precise trigger function. This is particularly useful for the pretrigger recording mode.

The trigger function is probably the most important recording control function in the unit. Careful and correct use of this function is required in order to realize the full performance of the unit. The trigger detection circuitry along with its attendant delay can be used to start or stop the recording process depending on the record mode selected.

The trigger can be provided automatically with the selection of the "Auto" trigger mode. This operation will cause alternating record and display sweeps and is normally useful only during check-out of the instrument or set-up of an experiment.

A trigger function must be provided in either Single or Normal trigger modes. Single trigger operation is described above in the discussion of the arm function. In Normal trigger mode, a trigger function is required for each record cycle but no arm signal is needed.

The trigger circuitry in the Model 1015 is very versatile. The trigger event can be derived internally from any one of the input signals or from a separate external input signal. The detection threshold is adjustable over twice the input range set on the selected input channel or ±10 volts when the external input is selected. More than one internal channel may be selected to provide the trigger function. In this case the trigger will be selected from the input signal which first satisfies the level and slope criteria of the trigger. When more than one internal source is selected, the level sensitivity is reduced. If two

channels are selected the sensitivity is reduced to 1/2 that for only one and when three sources are selected the trigger level sensitivity is only 1/3 the single source value. Positive or negative trigger slope is selectable as well as AD or DC coupling.

The end-of-sweep function, or the EOS function as it is sometimes abbreviated, occurs after the memories have been refreshed once. With the Model 1015 set for four channel recording, the EOS function will occur after 1024 sample intervals. Similarly EOS will occur after 2048 sample intervals in two channel operation, or after 4096 sample intervals in single channel configuration.

3.33 Modes of Operation

The record sequence in the Model 1015 is determined by the record mode selected and the choice of single or dual timebase recording. Two basic record modes are provided. They are called delayed mode and pretrigger mode. The timebase function selection and the record mode selection provide four basic record cycles under the control of the arm, trigger and End-of-Sweep (EOS) events. These four record control relationships are illustrated graphically in Fig. 3.2.

3.331 Delayed Sweep Mode, A Only Timebase

In the delayed record mode with single time base, the record cycle is initiated by the delayed trigger, and it is ended at the end-of-sweep (EOS). This recording function can be used in various ways depending on the setting of the trigger delay. With the delay set to zero, a straight forward normal sweep mode is produced. With the trigger delay set to a significant value, delayed sweep operation is produced. The delayed sweep mode of operation is used in situations where the only good trigger signal precedes the data to be recorded. In many cases the delay between the trigger and the desired information is greater than one sweep time. In these cases the signal would not be recorded with sufficient resolution to be useful. By delaying the initiation of the sweep with the trigger delay and sampling the signal at a faster rate, the information can be recorded with good time resolution.

3.332 Pretrigger Mode, A Only Timebase

Pretrigger recording is a unique feature of Biomation Waveform Recorders. Pretrigger recording allows the capture or recording of signals that are not known to be significant for recording until after the signal has occurred. Another good use of this mode is in cases where the only good trigger available follows the information of interest.

In the delayed recording mode the memories are filled with new information when the trigger occurs, or later. In the pretrigger recording mode of operation the memories are continuously being updated after the unit has been "armed" and will discard information (from the "other end" of the memories) at the same rate. When the trigger occurs, the recording function ceases after the selected trigger delay time. If the trigger delay is zero, the memories will contain the information for the signals which occurred for one complete sweep time prior to the trigger. The delay set on the trigger delay in this mode will determine which portion of the signal in the memory occurred after the trigger. Thus, any portion of the sweep time can be set to occur before or after the trigger event in the pre-trigger record mode of operation by simply adjusting the trigger delay setting. Figure 3.3 and 3.4 illustrate the advantage of utilizing the pretrigger recording mode.

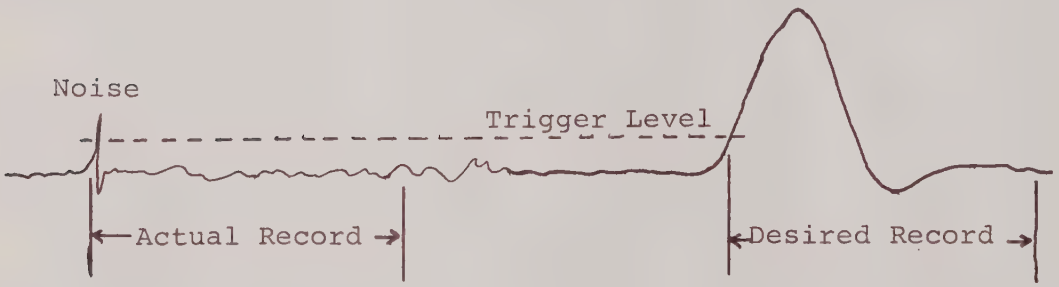


Figure 3.3 The effect of noise with a conventional trigger circuit.

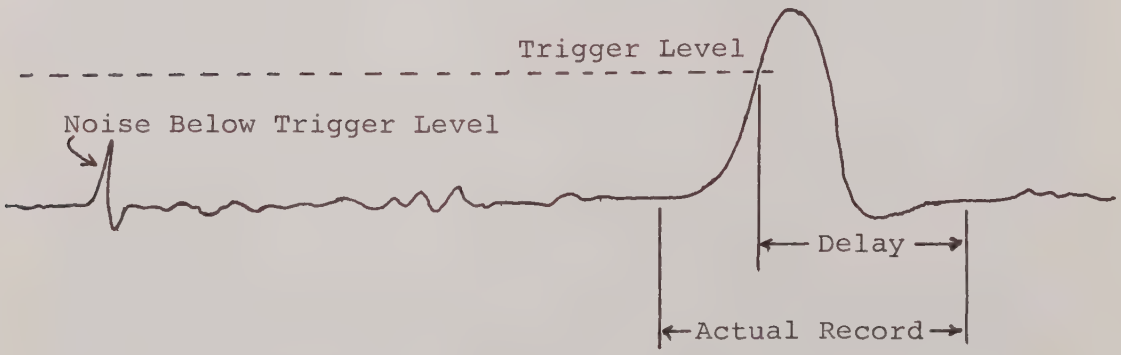


Figure 3.4 The manner in which Pretrigger Recording ensures the capture of significant prior event information.

3.333 Dual Timebase Operation

The dual timebase operation of the Model 1015 permits the recording to begin at one sweep rate and conclude with a different sweep rate, i.e., sampling of the input signals in the dual timebase mode begins with sample intervals at one linear rate and switches to sample intervals at another linear rate for the conclusion of the recording period. The point at which the switching occurs is dependent upon the front panel control settings and the record mode selected as described in the succeeding paragraphs.

3.334 Delayed Sweep Mode, Dual Timebase

This mode of recording permits the recording of an input signal with portions of the signal recorded at two independent rates. This is particularly useful in studying waveforms which contain fast and slow components. The point at which the record rate switches from the first sweep rate to the next is determined by the setting of the trigger delay. Thus, recording is initiated by the trigger, the rate is changed by the delayed trigger, and the recording is terminated by the EOS.

3.335 Pretrigger Mode, Dual Timebase

This mode is essentially the same as the pretrigger record mode described above with the addition of the switching of the record rate by the trigger. This mode is very convenient for recording at a slow rate a long period of time (but relatively few samples) prior to a trigger event, and then recording at a rapid rate (good time resolution) the signal occurring after the trigger event.

3.4 Data Acquisition Precautions

The Model 1015 is basically a digital recorder. The user should not overlook this fact because, by its very nature, the digital approach to signal storage has particular characteristics. There are some conditions under which these characteristics can seriously affect the quality of the information stored. This section will deal with these performance factors.

3.41 Sampling Rate

The sampling theorum states that the sampling rate must be at least twice the highest input frequency to be measured. In practical situations any complex waveform, such as a sine wave, should have at least four data points throughout the full cycle in order to realize a good reproduction of the original waveform. The sampling theory can easily be demon-

strated by taking a high frequency continuous signal, such as a sine wave, and operating the Model 1015 through all of its available sample rates. It will be observed that at slow rates a very respectable signal can be obtained which bears little direct relationship to the input signal. This mixing phenomena can be avoided by the use of the proper sample rate or with an external low pass filter to limit the high frequency components in the input signals.

3.42 Output Smoothing

The digital information coming out of the Model 1015 memory goes through a smoothing digital-to-analog converter. This converter makes the output appear to be a somewhat continuous trace rather than a series of points normally expected from a digital instrument. While this smoothing does filter out a major portion of the sample frequency which was added in the sampling process when the signal was recorded, further filtering can be added to further improve the reconstruction fidelity.

3.43 Amplitude Resolution

The Model 1015 converts all analog input signals to digital words of 10 binary bits each. This means that the amplitude resolution is 1 part in 1024, or 0.1% of the full scale amplitude. Note that resolution does not imply an accuracy specification. Resolution is 0.1%; accuracy depends on resolution, drift, gain tolerance, signal slew rate vs A/D aperture, and amplifier bandwidth, among other things.

SECTION IV

Operation

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, setup procedures prior to using the Model 1015, and step-by-step operating procedures for various modes of operation. A thorough understanding of this section is essential to the successful use of the instrument.

4.2 Front Panel Controls and Connectors

4.21 Arrangement of Controls

The controls of the Model 1015 are arranged in five groups of controls, according to function. Figure 4.1 shows the front panel. The five groups of controls are as follows:

Input Controls, Channels 1 thru 4

Record and Input Modes

Trigger

Time Base

Display/Mode and Output

4.22 Unique Switch Types

Two rather unique types of switches are used on the front panel: the lever switch, which is a variation of the thumbwheel switch, and the alternate action pushbutton.

The lever switch, used for Trigger Delay settings, is adjusted merely by moving the lever up and down. The detents are positive and easy to feel.

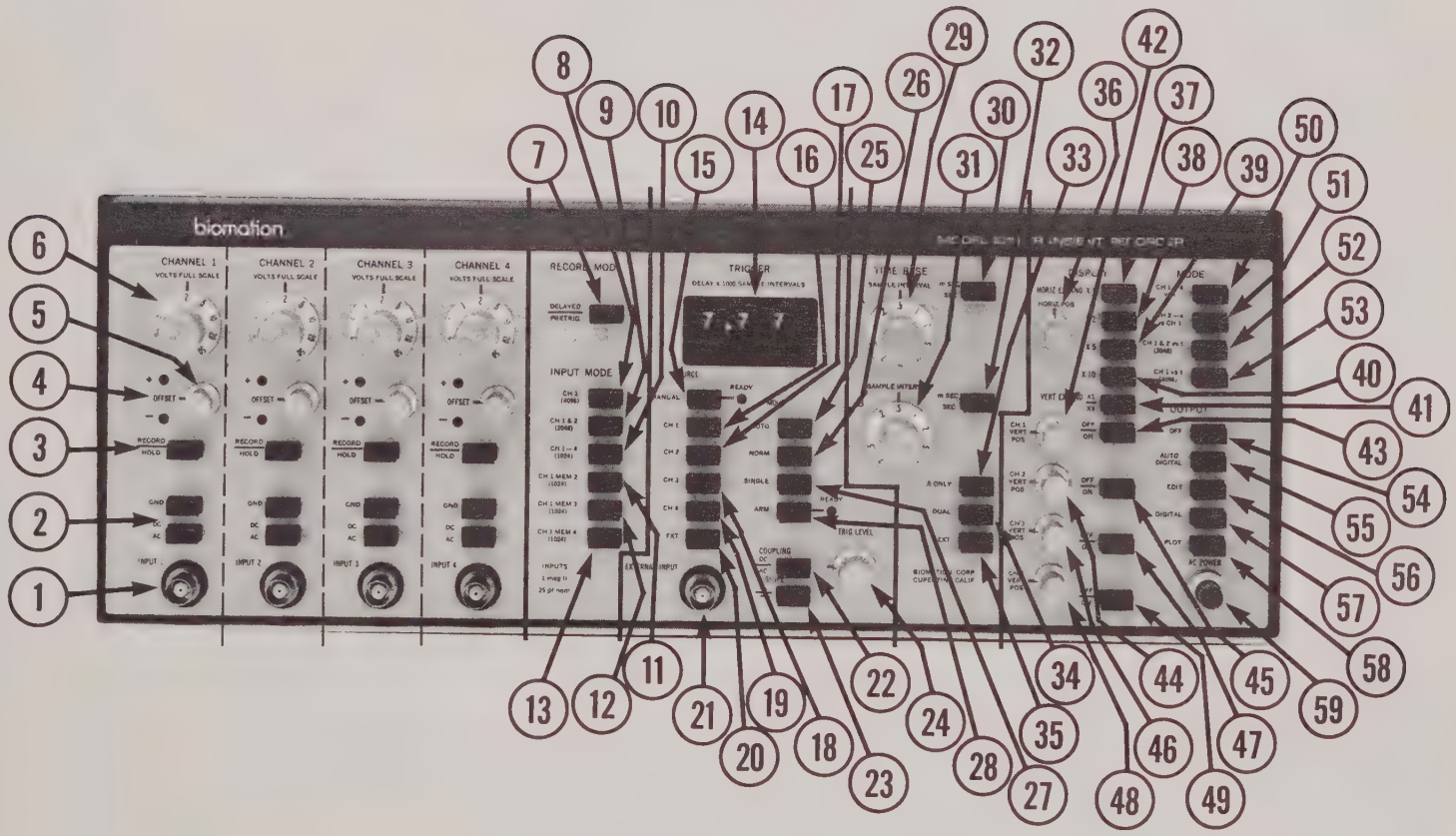


Figure 4.1 Front Panel Functions

The alternate action pushbutton, by pressing it, latches in the "in" position. It is released by pressing it again. The legends associated with the alternate action switch are observed as follows: there are two words beside each switch, separated by a horizontal line. The switch selects the upper function when in the "out" (unlatched) position, and selects the lower function when in the "in" (latched) position. To summarize: upper function, button out; lower function, button in.

4.23 Input Controls

There are four identical sets of controls in this group, one for each channel. The explanation of one set applies to each of the other sets.

(1) Signal Input Connector

Impedance 1.0 megohm in parallel with 50 picofarads to ground. BNC connector.

(2) Coupling Switches

DC (out) and AC (in). AC coupling provides 3db cutoff at 1.6 Hz. GND (in) disconnects the Input Connector from the input amplifier and grounds the input to the amplifier.

(3) Record/Hold

Record (out) enables a signal to be applied to the input and to be recorded into memory, discarding the previous information. Hold (in) allows a signal to be applied to the input but not recorded, thereby "holding" the previously recorded information. This manual Record/Hold selection is useable when the Record Mode is selected to be CH1-4 (1024), see 11 below.

(4) Offset Indicators

These LEDs tell the operator when the input signal exceeds the positive or negative full scale of the instrument, as set by the Offset and Volts full scale controls.

(5) Offset Control

This potentiometer allows the user to adjust the internal baseline of each input to permit use of the full dynamic range with unipolar signals or compensate for DC levels in the input signal. The offset can be set to the negative or positive full scale of the input range. The Offset Indicators, described above, aid in the adjustment of this control.

(6) Volts Full Scale

This nine position switch selects the full scale range, in a 1-2-5 sequence, of the instrument. The full scale sensitivity is step-variable from a maximum of 100mV (±50mV with no offset) to 50V (±25V with no offset). For all voltage ranges, the analog bandwidth is 25kHz.

4.24 Record and Input Modes

(7) Delayed/Pretrig

Delayed (out), Pretrigger (in). Sweep and Pretrigger Delay are adjustable in 10 word increments using Trigger Delay (14).

(8) CH 1 (4096)

(In; interlocked with switches (9) thru (13)). Provides one channel recording with 4096 words of memory.

(9) CH 1 & 2 (2048)

(In) Provides two channel recording with 2048 words of memory per channel.

(10) CH 1-4 (1024)

(In) Provides four channel recording with 1024 words of memory per channel.

(11) CH 1 MEM 2 (1024)

(In) Permits routing an analog signal through the input and A/D circuitry of Channel 1, but loading the digitized signal into the memory of Channel 2. The Record/Hold switch for Channel 2 must be in the Record position (out). The Record/Hold switches for Channels 1, 3 and 4 have no effect.

(12) CH 1 MEM 3 (1024)

(In) Permits routing an analog signal through the input and A/D circuitry of Channel 1, but loading the digitized signal into the memory of Channel 3. The Record/Hold switch for Channel 3 must be in the Record position (out). The Record/Hold switches for Channels 1, 2 and 4 have no effect.

(13) CH 1 MEM 4 (1024)

(In) Permits routing an analog signal through the input and A/D circuitry of Channel 1, but loading the digitized

signal into the memory of Channel 4. The Record/Hold switch for Channel 4 must be in the Record position (out). The Record/Hold switches for Channels 1, 2 and 3 have no effect.

4.25 Trigger

(14) Trigger Delay X1000 Sample Intervals

This lever switch permits adjustment, in 10 sample increments to 9990 samples, of sweep and pretrigger delay. The amount of delay is determined by the internal sample interval set on the Time Base switches (29-32) or the external Time Base (35). When switch (7) is in Delayed Record Mode (out), this delay is between the detected trigger (internal or external 16-20) and the time recording begins. When switch (7) is in Pretrig (in), the delay is between the detected trigger and the end of recording. This switch also controls the point during record, at which the time base changes speeds. See also description of switches (31), (32), and (34).

4.251 Trigger Source

(15) Manual

Permits manual triggering of the instrument whenever the Ready light is on.

(16) CH1

(In; interlocked with switches 17, 18 and 19, however, more than one can be depressed together). When CH1 is selected, the unit obtains its trigger from the analog signal that passes thru Channel 1.

(17) CH2

(In) Depressing this switch permits the unit to be triggered from the signal passing thru Channel 2.

(18) CH3

(In) Depressing this switch permits the unit to be triggered from the signal passing thru Channel 3.

(19) CH4

(In) Depressing this switch permits the unit to be triggered from the signal passing thru Channel 4. Note: Switches 16, 17, 18 and 19 may be depressed simultaneously; this permits the unit to trigger on

any of the four channels, whichever signal exceeds the threshold first. However, the trigger sensitivity is decreased by a factor of 4 with respect to the single channel sensitivity. If two buttons are depressed, then the trigger sensitivity is decreased by a factor of 2, etc.

(20) EXT

(In) Depressing this switch allows the unit to accept an external trigger signal via the front panel External Trigger Input.

(21) External Input

This BNC connector permits the application of an external signal to trigger the unit. Switch (20) must be depressed to use this input. Input impedance: 1.0 megohm in parallel with 50 picofarads to ground.

(22) Coupling

Provides DC (out) or AC (in) coupling for the trigger signal for either the internal or external sources.

(23) Slope

Selects positive (out) or negative (in) slope triggering for either the internal or external trigger signals.

(24) Trigger Level

This control provides trigger level adjustment within the range of 2 X full scale (as set on switch (6)) on internal trigger, or ±10V when applying an external trigger signal.

4.252 Trigger Mode

(25) Auto

When this switch is depressed, the unit will arm and trigger itself at a fixed rate. This operation is normally useful for equipment checkout or system set-up adjustments.

(26) NORM

In this mode, the unit arms itself automatically but must be triggered by a subsequent event from either an external or internal source. A trigger event will cause signals applied to the selected inputs to be recorded

and stored until the next trigger event when new signals will be stored, and the previously stored signals erased.

(27) SINGLE

This mode requires that, for each record cycle, the Arm button (28) be depressed, or an Arm signal be applied to the Arm input (1) on the rear panel to allow the unit to accept a subsequent trigger event.

(28) ARM

Permits manual arming of the unit when the Ready light is on.

4.26 Time Base

(29) Sample Interval A

Rotary switch for the selection of the time interval between samples, in a 1, 2, 5 sequence. Used in conjunction with switch (30) to provide a range of sample intervals between .01 milliseconds and 10 seconds.

(30) mSEC/SEC

Multiplier for switch (29). Gives milliseconds (out) and seconds (in).

(31) Sample Interval B

Same as switch (29), except this switch controls the alternate time base when switch (34) is depressed.

(32) mSEC/SEC

Same as (30), except this switch operates with switch (31).

(33) A ONLY

The unit will operate only at the sample interval selected on switch 29.

(34) DUAL

This permits the unit to operate in the dual time base mode during the recording of a signal. Switches (29-32) control the two sample intervals desired and switch (14) controls the point at which the unit switches from Sample Interval A to Sample Interval B.

(35) EXT

Permits the application of an external signal to control the record rate. This signal is applied to the rear panel Time Base In BNC connector. If the frequency is less than 1kHz, set switch (30) to SEC (in). If the signal frequency is 1kHz or greater set switch (30) to mSEC (out) and set switch (29) to position .01, .02, .05, .1, .2, .5 or 1.

4.27 Display

4.271 Horizontal Display

Note: These controls produce the described display action only when the X output from the 1015 is properly input to the CRT. These controls also produce the same relative action on the Plot output signals.

(36) HORIZ POS

Controls the position of the display on the CRT face.

(37)
(38)
(39)
(40) HORIZ EXPAND X1, X2, X5, X10

These switches control the expansion of the sweep, and therefore the number of points displayed on the CRT. For example, when in the four channel mode, X1 (in) permits viewing all 1000 points stored in each memory. By depressing X10, 100 points per channel at a time may be viewed by operating the HORIZ POS control.

4.272 Vertical Display

Note: These controls also operate on the Plot output signals.

(41) VERT EXPAND X1/X4

This switch permits each signal to have a full scale vertical amplitude of 1/4 the display, X1 (out), or an expansion by a factor of 4, X4 (in), so that the entire CRT can be filled with the output of one channel.

(42) CH1 VERT POS

Controls the position of Channel 1 display information on the CRT face.

(43) OFF/ON

Permits turning off (out) or on (in) Channel 1 display information.

(44)
(45) Same as above, but for Channel 2.

(46)
(47) Same as above, but for Channel 3.

(48)
(49) Same as above, but for Channel 4.

4.28 Mode and Output

4.281 Mode

Note: These switches also operate on the Plot output signals.

(50) CH1-4 vs t

(In; interlocked with switches (51), (52) and (53). This switch provides four sweeps on the CRT of approximately 1K words per sweep. Provides a meaningful display in conjunction with record mode switch (10).

(51) CH2-4 vs CH1 (in)

This switch provides true "X vs Y" display, by plotting the display signals of Channels 2, 3 and 4 (on the vertical axis) versus the display signal of Channel 1 (on the horizontal axis).

(52) CH1 & 2 vs t (2048) (in)

This switch provides two sweeps on the CRT with approximately 2K words per sweep. Provides a meaningful display in conjunction with record mode switch (9).

(53) CH1 vs t (4096) (in)

This switch provides one sweep on the CRT of approximately 4K words. Provides a meaningful display in conjunction with record mode switch (8).

4.282 Output

(54) OFF

(In; this switch interlocked with switches (55) and (56)).

This switch causes the unit to revert to the display mode at the end of record, with no digital or plot data available.

(55) AUTO DIGITAL (in)

This switch causes the unit to revert to the digital output mode after completion of a record sweep, at which time the first word is available at the digital output connector (13) on the rear panel. Display and Record are inhibited until the entire memory contents (4096 words) have been output, the output is terminated by digital input to rear panel interface, or switch (54) is depressed.

(56) EDIT (in)

This switch provides an output standby mode, wherein after record, a display output is provided. If, after viewing the display, it is desired to output the data, the DIGITAL (57) or PLOT (58) buttons may be pressed to initiate the output of the data.

(57) DIGITAL

This button manually initiates the digital output of data in EDIT output mode. Display and Record are inhibited during the output of data as in AUTO output mode. Digital output may be re-entered repeatedly, but each time Digital Output is entered, the output begins with the first memory word.

(58) PLOT

This button initiates the output of analog data to a plotter when EDIT mode is used. The Display and Mode Controls act upon the plot output signals as follows:

1. Horizontal and vertical positioning of the signals is available from controls (36) and (42), (44), (46) and (48) respectively.

2. Horizontal and vertical full scale amplitude of the signals is selectable from switches (37), (38), (39), (40) and (41) respectively.

3. The signals in Channel 1, 2, 3 and 4 will be plotted automatically in sequence as selected by switches 50-53. Individual plot outputs of each recorded signal can be selected by using switches (43), (45), (47) and (49).

(59) AC POWER

An illuminated alternate action switch indicates AC Power on.

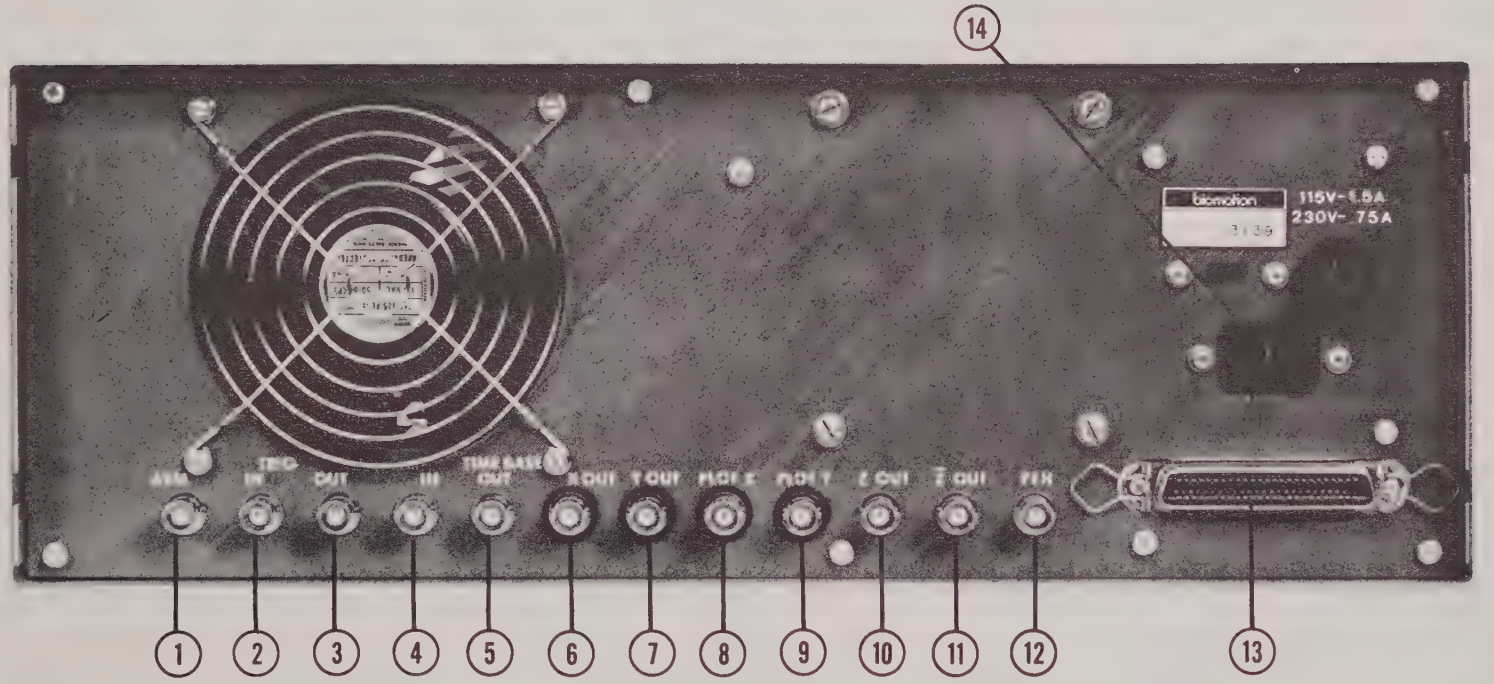


Figure 4.2 Rear Panel Functions

4.3 Rear Panel Connectors

Figure 4.2 shows the rear panel connections.

4.31 Synchronizing Connections

Multiple 1015 units may share the same ARM and TRIGGER commands. The ARM (1) and/or TRIG IN (2) and TRIG OUT (3) connectors of the units can be interconnected. The units may then all be armed at the same time with a common external signal, with the appropriate waveshape, driving the "arm line."

The TRIG IN (2) connector of one unit will accept the TRIG OUT (3) signal of another unit so that essentially simultaneous triggering may be realized. The unit that is accepting the Trigger signal should have switch (20) depressed.

To provide the same time base for recording, TB IN (4) and TB OUT (5) are utilized. TB OUT from one unit provides the time base signal, via TB IN to the other unit.

4.32 Display Outputs

X OUT (6)

A repetitive sweep ramp of 1 volt peak, switch selectable to 2, 5, and 10 volts (sweep expand) and switch selectable durations of 1 msec (4-trace display) 2 msec (2-trace display) and 4 msec (1-trace display). Or, selectable as repetitive signal from channel one to produce X vs Y displays with respect to channel 2, 3 and 4 signals. Origin adjustable ±0.5 full scale (position control).

Y OUT (7)

A repetitive sequential replica of all recorded signal(s), 0.25 volts full scale, switch expandable to 1.0 volts. Reconstruction rate 1 μsec per word. Each signal selectable Display or Off with individual vertical position controls coordinated with X output selection. Vert positions adjustable ±2X full scale.

4.33 Blanking Voltages

Z OUT (10) and $\overline{Z}$ OUT (11)

Provide signals for retrace blanking or oscilloscope trigger. Z OUT is a TTL voltage level from 0 to +5V (nominal) at the start of the display period. It stays positive during X sweep and returns to 0V during retrace. $\overline{Z}$ OUT is held at 0V during display and goes to +5V during retrace.

4.34 Plot Outputs

PLOT X (8)

Provides, on initiation of Plot output a sweep ramp of 1 volt peak, switch selectable to 2, 5 or 10 volts (expanded) and switch selectable durations of 100 sec (1000 point plot), 200 sec (2000 point plots) and 400 sec (4000 point plot). Or selectable as 100 sec plot of signal from channel one to produce X vs Y plots with respect to signals in channels 2, 3 and 4. Origin adjustable ±0.5 volts.

PLOT Y (9)

Provides, on initiation of Plot output, the analog replica of the recorded signals at a rate of 0.1 seconds per point (100 seconds for 1000 points). Channels sequentially plotted or individually selectable. Selectable 0.25 volts or 1 volt full scale. Position bias individually set for each channel ±0.5 volts.

PIN (12)

This output provides for pen lift and/or recorder start. The signal goes true (+5V) at the start of the plot cycle and returns to zero after the cycle is complete. Optionally available true when not plotting or as a positive or negative 1ms pulse.

Digital Interface (13)

Details of this connector, including pin assignments are given in Section 5, Digital Interface.

4.34 AC Line Connector, Fuse holder, and Line Voltage Selector (14)

The connector housing contains a line filter. Note the fuse ratings printed on the rear panel (1.5A for 115 V, .75A for 230 V). When changing line voltage, ensure that the proper fuse is used. The line voltage selector may be changed using a small screwdriver. Leave line cord unplugged while changing fuse and selector.

4.4 Set Up Procedure

4.41 Initial Set Up

This section describes the connection of a Model 1015 with a CRT display or oscilloscope and the steps to record and display a known signal.

Before connecting the unit to line power, check the voltage selector switch on the rear panel to ensure that it is set to the proper line voltage and be sure that the correct size fuse (as printed on the rear panel) is installed.

Connect the Model 1015 to a pulse generator and CRT display as shown in Figure 4.3a or 4.3b. It may be necessary to use the $\overline{Z}$ output of the 1015 for the retrace blanking signal as CRT drive circuitry varies greatly in the polarity of this input.

CAUTION - Some older "tube type" oscilloscopes have a high voltage on their Z axis inputs. THIS COULD DAMAGE THE Z or $\overline{Z}$ OUTPUT OF THE 1015.

Set the oscilloscope and pulse generator as follows:

Vertical sensitivity	0.1V/div., DC coupled
Vertical position	Middle of display
Horizontal sweep	0.1 ms/div. (Fig. 4.3a)
Horizontal sensitivity	0.1V/div., DC coupled (Fig. 4.3b)
Trigger input	-, DC coupled, external (Fig. 4.3a)
Pulse Generator	100Hz pulse rate, 2msec wide, 0 to +1V pulses

Set the Model 1015 as follows:

CHAN 1

COUPLING	DC (OUT)
GND	OFF (OUT)
RECORD/HOLD	RECORD (OUT)
OFFSET	Negative (bottom)
VOLTS FULL SCALE	1
RECORD MODE	Delayed (out)
INPUT MODE	CH 1-4 (1024) (in)

Trigger

Delay	0.00
Source	CH1 (in)
Mode	NORM (in)
LEVEL	slightly positive
COUPLING, SLOPE	DC (out), + (out)

Time Base

Sample Interval A	.01
mSEC/SEC	mSEC (out)
A ONLY	in

Display

HORIZ Expand	X1 (in)
Vert Expand	X1 (out)
CH1 OFF/ON	ON (in)
All others OFF (out)	

Mode

CH 1-4 vs t	in

Output

OFF	in

A repetitively recorded pulse of about 2 divisions high and 2 divisions wide on the left end of the trace should be displayed on the CRT. Changing the TRIGGER MODE from NORM (in) to SINGLE (in) should cause the repetitive recording to cease. This will be evidenced by a slight brightening of the display trace and the ARM READY light should come on. If these actions do not occur, carefully check the controls per the above settings and the integrity of the CRT performance.

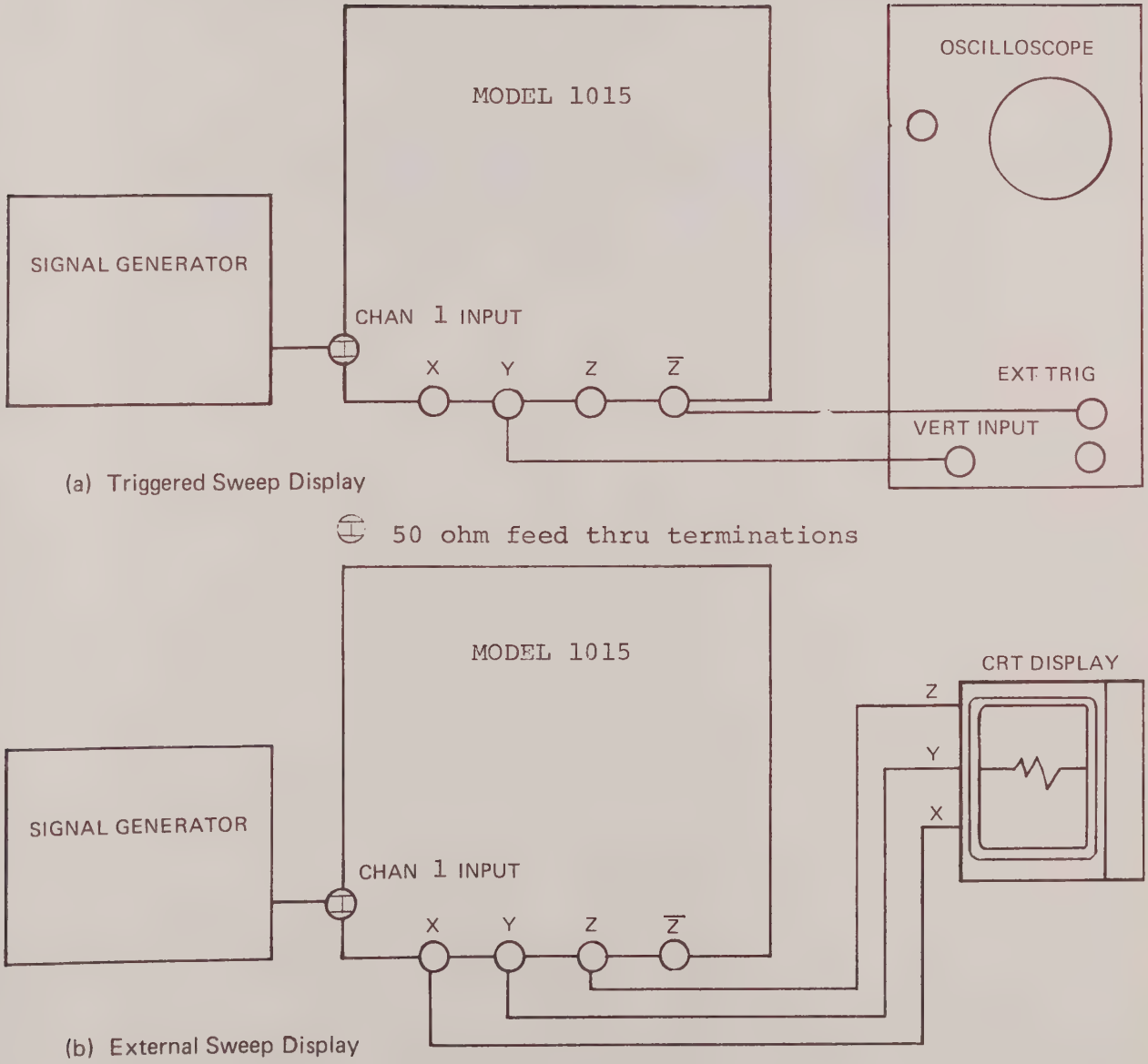


Figure 4.3 Display Interconnections

4.5 Operating Procedures

In this section several modes of operation will be discussed and illustrated. A pulse generator capable of generating a single pulse upon manual command and able to drive a 50 ohm load is required. Terminate the generator line at the input connector of the 1015 with a 50Ω feedthru termination. Set the generator to give repetitive pulses 2ms wide, going from 0V to slightly over +1V and occurring at a 500Hz rate.

4.51 Normal Mode

Set the Model 1015 and oscilloscope exactly as described in Section 4.41 above. The + OFFSCALE lamp will be lit. Reduce the amplitude of the input pulse to just under +1V. The + OFFSCALE light should go out and the display should resemble Fig. 4.4

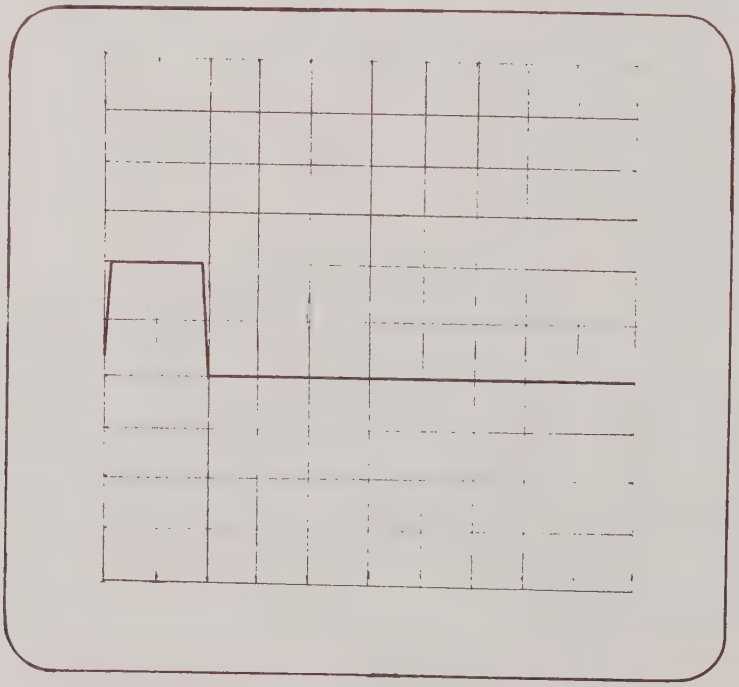


Figure 4.4 Measurement Signal

4.52 Pretrigger Mode

Make the following changes in the control settings:

Record Mode	Pretrigger (in)
Trigger	
Delay	1.50

Observe the display, it should look like Fig. 4.5. One pulse of the repetitive waveform is being recorded and displayed before the next pulse comes along. The significant thing here is that one can observe 500 samples (in this example) of prior trigger event input signal, and 500 samples of after trigger detection signal.

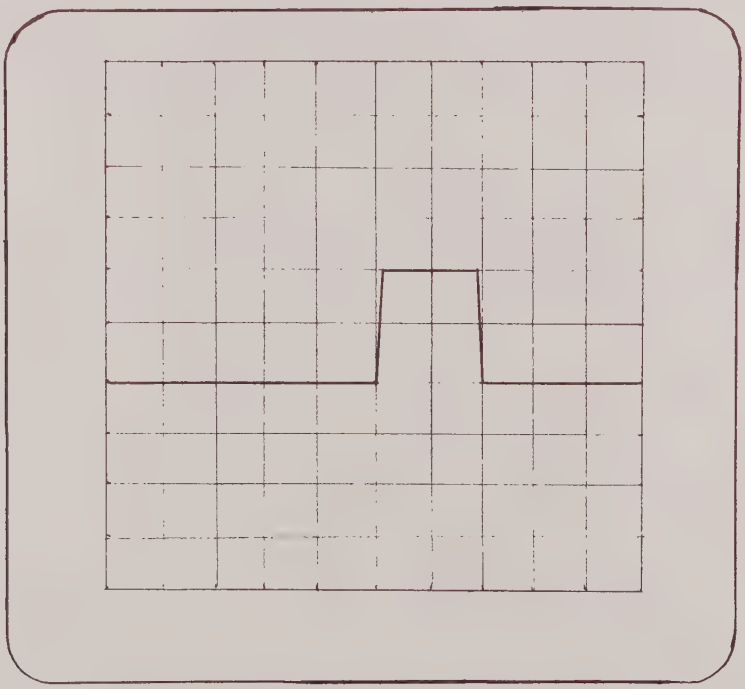


Figure 4.5 Pretrigger Recording
Illustrating about one-half of recorded signal contains prior trigger event data.

Note: In Pretrigger Recording, recording begins when the unit is armed and terminates when the Trigger Delay has run out. If no Trigger Delay has been set in, the unit will terminate recording as soon as it detects a trigger, and the following signal will not be recorded. Observe the effect of Trigger Delay by switching through the range of Trigger Delay on the first digit to the right of the decimal point. At 0.00, the pulse will disappear to the right of the CRT. At 0.90, the pulse wavefront will be spaced 100 samples from the left edge of the CRT.

To further illustrate the significance of pretrigger recording, change the pulse generator controls so that a single pulse can be manually strobed out. Depress the Trigger Mode Single switch. Observe that the Trigger Ready light is on. Pulse the generator. The Trigger Ready light will go out and the Arm Ready light will come on. The display will be as Figure 4.5, except that there will be no flicker.

With the pulse stored in memory, observe that using the HORIZ and VERT EXPAND and position controls, the pulse may be studied using up to X10 magnification horizontally, and X4 vertically. The range of control is such that the pulse may be stored anywhere within the memory, and still be fully examined.

4.53 Dual Time Base Mode

Return the RECORD MODE to Delayed (out) and TRIGGER to Normal (in) and Trigger Delay to 0.10. Return the pulse generator to the 500Hz pulse rate.

Set Time Base B to .1mSEC (out), and depress Dual. On the CRT, observe one wide pulse, followed by 10 narrow pulses.

In this Mode, the Trigger Delay determines the point at which the unit switches from Time Base A to B.

4.54 X vs Y Display

A function generator will be used to illustrate this mode.

Switch to A ONLY (in) Time Base, Trigger Delay to 0.00 and turn on the remaining three traces. The following procedure will be used to load a sinusoidal signal into each of the four memories:

1. Set Trigger Mode to Single

2. Connect the function generator to INPUT 1 and set for 100Hz, 1Vpp sine wave out. Depress Arm button. This stores the signal in the memory of Channel 1.

3. Adjust the generator to 200Hz. Depress CH1 MEM 2. Depress Arm. This store a 200Hz signal in Channel 2.

4. Adjust the generator to 300Hz. Depress CH1 MEM 3. Depress Arm. This stores a 300Hz signal in Channel 3.

5. Adjust the generator to 400Hz. Depress CH1 MEM 4. Depress Arm. This stores a 400Hz signal in Channel 4.

Depress Display Mode switch CH 2-4 vs CH 1. On the CRT, observe three lissajous patterns, the result of presenting the analog signals stored in Channels 2, 3 and 4 versus the signal stored in Channel 1.

SECTION V

Output Interface

5.1 Introduction

The Model 1015 provides a versatile and comprehensive analog and digital output interface. This interface is designed to be especially convenient for presentation of the recorded signals on a CRT display, for analog output of these signals at a slow rate to a strip chart or X-Y recorder and for transfer of the digital data to digital computers or mass storage devices.

The operation of the Model 1015 with a CRT display or oscilloscope is described in sections 4.4 and 4.5. Operation of the unit with analog plotter is described below and the detailed description of the digital interface is also presented in this section.

The digital output is effected via a bit-parallel, word-serial data exchange. The versatility of this interface is enhanced by a pin in the interface connector which allows the user (or system designer) to assign the logical definition of the data output "word". This is readily done by a ground strap on the mating connector. The digital interface connector also contains three pins for assigning the "address" of the unit. Thus, a number of units can be connected in parallel on a digital "bus" and individually controlled.

5.2 Plotter Interface

The plot output of the Model 1015 can be initiated by pressing the Plot pushbutton located on the front panel, when EDIT output mode is selected. During plot output the Model 1015 changes from the high speed display clock rate of 1μsec/word to a slow speed clock rate of 0.1 sec/word. This output rate will require 102.4 sec for plotting a 1024 word signal. The X and Y plot outputs are grounded to prevent recorder chatter when not plotting. During the plot operation the Y plot output signal has the same characteristics as the Y output signal (but at the slower rate). Similarily the X plot output has the same characteristics

as the X display output but at the slower rate. The plot outputs are filtered to provide a smooth trace. A pen signal is available at the rear panel for use with the plotter. This signal goes high (+5V) during plot but is otherwise at 0V.

5.21 External Plot Time Base

The normal plot rate is determined by an internal 0.1Hz clock as described above. However, an external clock may be used to control the plot rate. The external plot rate signal should be a 0 to +4 volt pulse train and can be any rate up to 500Hz. This signal can be input to pin 12 on the interface connector and it will determine the plot rate whenever plot is selected in the normal manner as described above providing that the plot rate input is enabled by grounding pin 13.

5.3 Data Connector Definitions

The 50-pin rear panel connector provides the physical interface for digital data output. The connector is an Amphenol Micro-Ribbon 57-40500. The mating connector is an Amphenol part number 57-30500.

The pin assignments for the digital interface are listed in the following table:

Pin #	Mnemonic	Description	Input/Output
1-9	N/C	No Connection	-
10	OMS	Output Mode Start	I
11	N/C	No Connection	-
12	$\overline{\text{EPT}}$	External Plot Time Base	I
13	$\overline{\text{PTG}}$	Ext. Plot Time Base Enable	I
14	ADA	Address Input A	I
15	ADB	Address Input B	I
16	ADC	Address Input C	I
17	CMD	Word Command	I
18	$\overline{\text{FLG}}$	Output Flag	O
19	$\overline{\text{OMD}}$	Output Mode Stop	I
20	APA	Defines Address A	-
21	APB	Defines Address B	-
22	APC	Defines Address C	-
23	ODP	Defines Data Logic	-
24	ODA	Output Data 2^0 (LSB)	O
25	ODB	Output Data 2^1	O
26	ODC	Output Data 2^2	O
27	ODD	Output Data 2^3	O
28	ODE	Output Data 2^4	O
29	ODF	Output Data 2^5	O
30	ODG	Output Data 2^6	O
31	ODH	Output Data 2^7	O
32	ODI	Output Data 2^8	O
33	ODJ	Output Data 2^9	O
34	+5V	Five Volt Power	O
35	DOG	Output Status	O
36	RPR	Record Status	O
37-50	GND	Signal Ground	-

5.4 Digital Interface Signals

This section describes the electrical and timing characteristics of the input and output signals for digital output from the Model 1015.

5.41 Inputs

The logic inputs of the digital interface accept standard TTL digital signals (+2.4 to +5.0V high, 0 to +0.4V low) and present a load approximating that of one and one-half TTL gates, i.e., each input line requires a nominal current sink of 2mA to input a "low".

5.42 Outputs

The output data lines are only active when the unit is correctly "addressed". That is, the outputs do not present any signal nor place any load on the output lines unless the address code on the input address lines (pins 14, 15 and 16) corresponds to the code as programmed on the address definition pins (20, 21 and 22). Each of the output lines is capable of driving up to 30 standard TTL loads (maximum fan-out = 30). The data outputs will be positive or negative true (Pos or Neg logic), depending upon the connection to pin 23, (see below).

5.43 Logic Definition Connections

Logic Definition pins in the interface allow the user to define the "polarity" or "sense" of the digital output lines and to define the "address" to be assigned to the unit for digital control. Thus, the digital output bits (lines) can be assigned to be positive or negative true (Pos or Neg logic).

Positive true is defined to be the representation of a binary "one" by a positive (high) signal and the representation of a binary "zero" by a zero (low) signal. Conversely, negative true or negative logic is defined to be the representation of a binary "one" by a zero (low) signal and the representation of a binary "zero" by a positive (high) signal.

Positive true or positive logic signals are defined for the output data bits by leaving pin 23 open-circuited. Conversely, negative logic will be defined by connecting pin 23 to ground (pins 37-50).

The "address" that will be required in order to output digital data is defined by appropriate ground connections. For each "address" input bit that is to be recognized as "low", the corresponding address definition pin should be left open-circuited. Conversely, each "address" input bit that is to be recognized as"high" must have its

corresponding address definition pin grounded. For instance, if the desired address of the unit is to be "010" (assuming a positive logic convention), the address definition pin number 21 should be connected to ground denoting the "1" or high signal is to be recognized and pins 20 and 22 should be left disconnected. Note that positive or negative logic convention for the address is purely a matter of the definition of the convention used in describing the connections to the Logic Definition pins in terms of the logic to be used. Thus, if all three pins are left ungrounded (open), this defines an address of "000" using the positive logic definition and "111" when the negative logic definition is used.

5.44 Control Timing

Digital data transfer from the Model 1015 is regulated by two control signals: the output flag (FLG) signal and the input word command (CMD) signal. The FLG output signal indicates the output data status of the Model 1015. The CMD input signal initiates the fetch for the next data word.

In the following discussion, defining the FLG and CMD signals and their interrelationships, binary logic notation will be used, i.e., binary 0 (zero) and 1 (one) will be used to define the signals.

5.441 FLG level 1

When the FLG signal is a binary 1, a CMD can be input (0 to 1 transition) and it will be accepted. During digital data output, this FLG state indicates steady data is on the output lines.

5.442 FLG 1 to 0 transition

The 1 to 0 transition of the FLG signal denotes that the CMD input has been accepted. The CMD signal may be returned to 0, subject to a minimum "dwell" time of 100 nsec (see 5.446 below). During digital data output, this transition indicates that the process of fetching the next data word has begun.

5.443 FLG level 0

When the FLG signal is a binary 0, the unit is "busy" and no command signals (CMD 0 to 1 transitions) will be accepted. This normally indicates that the unit is busy fetching the next data word.

5.444 FLG 0 to 1 transition

The 0 to 1 transition of the FLG signal denotes that steady data is available to be "read" on the data output lines. The output data word is applied to the output data lines at least 50 nsec prior to this transition.

5.445 CMD 0 to 1 transition

Indicates that the output data word on the output data lines has been "read" and requests the next word.

5.446 Minimum pulse width

The minimum "dwell" time in either the binary 1 or 0 state for the CMD signal is 100 nsec. Narrower pulse width may result in failure of the unit to recognize the signal. Similarly, the FLG output signal will not be produced with binary 1 or 0 pulses of less than 100 nsec duration.

5.45 Output Data Rates

The signal data in the memory of the Model 1015 can be output asynchronously at rates up to 1×10^6 words/sec under the control of the FLG and CMD signals. The output rate is influenced by the internal clock frequency and the need to refresh the memory between output words at low read rates. The former is evidenced by a 1μsec latency in the output with respect to 1MHz synchronous clock. This latency does not reduce the average data rate of the unit but it does cause a cyclic "grouping" of the data which is particularly noticeable at rates near the maximum rate of 1×10^6 words/sec. For instance, at an average output rate of 0.75×10^6 words/sec, the words would be spaced in time by two 1μsec intervals followed by a 2μsec interval, then two 1μsec intervals, a 2μsec interval, etc.

As the digital memory in the Model 1015 is made up of MOS shift registers, the memory must be cycled periodically in order to prevent loss of data. Thus, protective circuitry is provided in the unit to detect the need for cycling the memory and cause this to occur during the digital output whenever the output rate is low. During the time that the memory is being cycled, no additional output data is available. This leads to an output latency period of up to the full memory cycle time (1ms) whenever the output rate is at or below 10KHz. This phenomenon is evidenced as follows: Average data rates are continuous from 1×10^4 to 1×10^6 words/sec. Data rates less than 1×10^4 words/sec will exhibit up to 1.0ms latency, e.g., if more than 100μsec. occurs between data request commands, a delay of up to 1msec will occur prior to the presentation of the next output data word. This latency will be evidenced by the FLG signal going low upon input of the subsequent CMD signal and remaining low for up to 1msec.

5.46 Memory Data Output Code

When the data in the digital memory of the Model 1015 is transferred to the digital output (under control of the

FLG signal and CMD signal), it is output in a pure binary code. The value represented by each word in the memory represents an instantaneous voltage level of the input signal and the input signal may be any value between zero and the full scale selected on the input attenuator (depending on the amount of input offset selected). Zero volts is represented by all "zeros" in the binary code and full scale volts is represented by all "ones". Thus, each LSB (least significant bit) represents one/1024th of the full scale voltage as set on the input attenuator.

5.47 Parallel Operation

The digital interface of the Model 1015 is arranged to facilitate the operation of up to eight like or similar units on the same set of digital I/O lines. This is done simply by connecting each line or bit in the digital interface of all of the units in parallel with the respective line in the controlling device. Each of the units can then be separately controlled by supplying its unique address (as assigned on each unit) along with the desired digital inputs to that unit.

Parallel operation of the Model 1015 is aided by the use of so-called "tri-state" logic driving all of the unit's digital data output lines. This type of logic presents essentially no load (or voltage) on the output lines when it has not been enabled by the specified "address" combination inputs. Thus, the output of paralleled units do not "fight" each other and no signal degradation is caused by the parallel connection. This is only true, of course, if all paralleled units have different assigned addresses. Identical addresses on two or more paralleled units will, obviously, cause contention.

The Model 1015 may be paralleled with similar devices which do not have "tri-state" output but use the more common "open-collector" logic for their digital output lines providing the common load resistor for the open-collectors on each output line is returned to +5V and the outputs of any of these units are arranged to "go high" when they are not "addressed".

5.5 Digital Output

The digital output can be initiated automatically or on demand by front panel or remote inputs, depending on the output mode selected (refer to the group of front panel controls labeled OUTPUT). The following statements describe the operation for each of the output mode conditions:

5.51 OFF

If the OFF output mode has been selected, no subsequent output of the digital data can be made unless another mode is selected. The unit will automatically switch to the Display mode at the end of recording. The Record Status output (pin 36) will indicate that recording is completed by transitioning from a one to a zero at the end of the record sweep. The OFF output mode prevents or stops digital or plot output but does allow the unit to accept an Arm or Trigger signal and execute a record cycle. This is useful because the 1015 is prevented from recording whenever it is in the process of plot or digital output.

5.52 AUTO DIGITAL

Selection of the AUTO output mode will cause the unit to automatically switch to the digital output mode at the end of the Record Cycle and the Record Status output will indicate that recording is complete as described above. Each word of the digital data is strobed through the output lines by the CMD and FLG signals as described in the preceding Control Timing discussion. With AUTO output mode selected, the first word of digital data from channel one will be presented on the output lines (assuming the unit is "addressed") within 1μsec after the end of recording and the 4096 words of data may be transfered across this interface with no delay. The data will be presented from memory one first, then memory two, memory three and memory four. During this process the unit will be prohibited from recording; thus, ensuring that the data will not be destroyed until it can be output. The digital output mode is only available once after each record cycle in this AUTO mode. Once the digital output mode is terminated with AUTO output selected no further data transfer of the data stored during the previous record cycle is possible except by switching to EDIT output mode (see below). The output mode may be terminated and the output reverted to Display (allowing a subsequent record cycle) in one of three ways. One, after all 4096 words have been clocked out, the digital output mode will automatically terminate. Two, the output can be manually switched to OFF thereby terminating the digital output mode. Or three, a negative transition from +5 volts to zero on the Output Mode Stop input (pin 19) with a minimum dwell time at zero of 100ns will terminate the digital output mode.

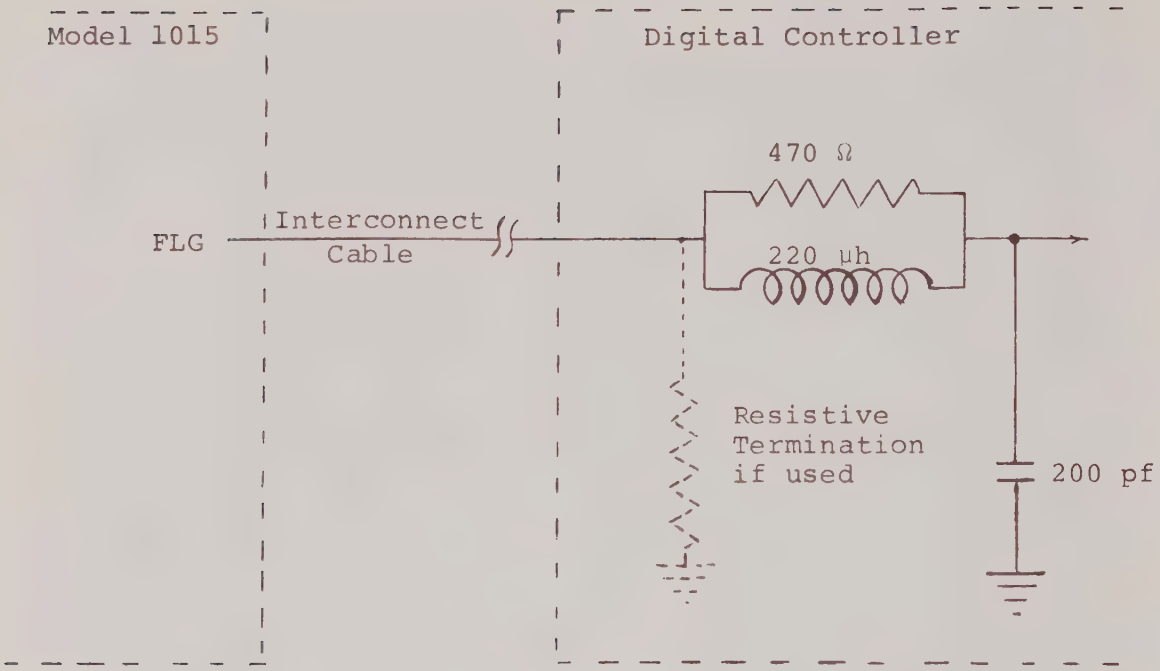
5.53 EDIT

Use of the EDIT output mode permits the user to observe the reconstructed signals in the memories on the display prior to the transfer of the data through the digital interface. With EDIT mode selected, the unit will go into Display mode after the end of the Record mode (denoted by the Record Status output). The digital output can be initiated by one of two ways: (1) by momentarily depressing the front panel Digital Output pushbutton, or (2) by inputting a 1.1msec pulse from +5 volts to zero and back to +5 volts on the Output Mode Start input (pin 10). Either of these two actions will cause the FLG signal to go to zero for a minimum of 100nsec and a maximum of about 1msec (depending upon the instantaneous relationship between the initiation signal and the Display cycle) and then the FLG signal will transition back to a "1", indicating that the first word in the memory is available on the output data lines. Subsequent words of the digital data are strobed through the output lines by the CMD and FLG signals as described in the Control Timing discussion above. Tne Output Status signal on pin 35 will also indicate by going high (assumming the unit is addressed) that the output mode has been established. (This signal will also indicate this information in the AUTO digital output described above.) The transfer of the data and the means for terminating the digital output in EDIT mode is the same as described above for AUTO but in EDIT mode the output of data may be re-established and repeated as many times as desired on the same data. In such an instance, the first word presented on initiation of the digital output mode will always be the first word in memory one.

5.54 Cable Parameter Compensation

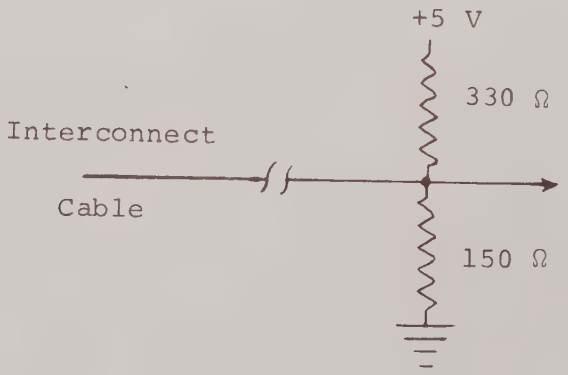
The Model 1015 is designed to facilitate rapid digital data transfer. For cable lengths up to about six feet between the Model 1015 and the digital controlling device, no special shielding, terminations or compensation is required on the data input or output lines. Any reflected signals, ringing and/or cross-coupling will normally be attenuated and "settled out" well within the 50nsec settling time delay between the output data and the FLG signal.

The FLG and CMD signals do, however, require some considerations in order to insure immunity from line ringing and/or cross-talk phenomenon. It is recommended that a simple filter be utilized on the Flag signal at the cable termination on the digital controller. The circuit shown in the following sketch has been found to be particularly effective for this use.



Cable lengths in excess of about six feet may require special considerations in order to insure error-free data transfer at high data rates. This is most easily accomplished by terminating the signal lines (twisted pairs) with 100 ohms.

The following recommended biased load network may be connected to each output line at the load end of the cable to provide a 100 ohm termination while preserving full fan-out (30 TTL) capability.



SECTION VI

Calibration Procedures

6.1 Calibration of Display Output

Adjustments are provided to calibrate X and Y display outputs to a specific display unit. Connect the unit as shown in Figure 4.3. Some X-Y displays such as the TEKTRONIX Model 604 and the DUMONT Model 1000 require a Zener diode clamp across the "X" input of the display to limit the X ramp to 3 volts. If this diode is not used, viewing of the complete stored waveform in the 5, 10, expand modes will not be possible. Install the Zener diode as shown in Figure 6.1

Figure 6.1 DIODE INSTALLATION

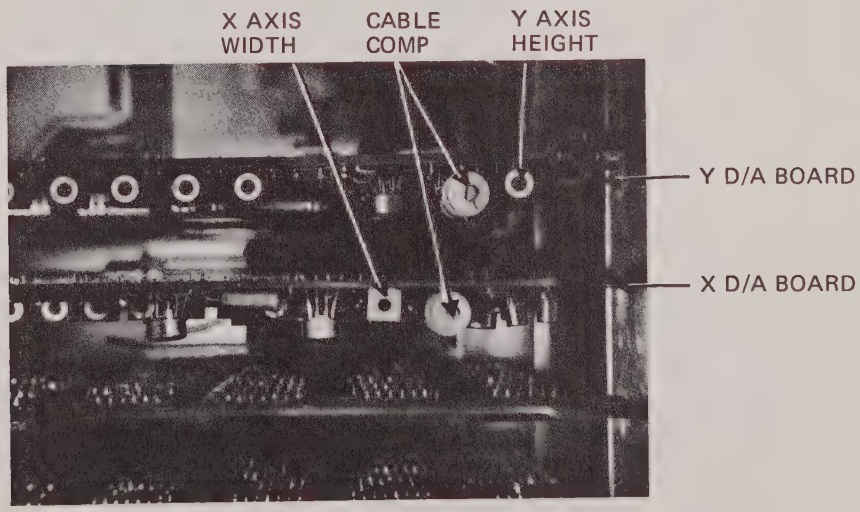


Figure 6.2 X and Y ADJUSTMENT CALIBRATE

1. With a greater than full scale signal displayed, adjust "Y-axis height" to give full scale display (adjustable from 0.8 to 1.2 V full scale in the X 4 position)

2. Adjust "X-axis width" to give full scale display. Be sure Display Expansion is in X1 position.

3. Adjust "Cable Compensate" for clearest square wave presentation.

6.2 Recalibration of the Internal Circuits

The following calibration procedures are intended to be used in recalibrating the internal circuits of the 1015. The entire instrument was calibrated before shipment and should not require any recalibration for at least six months.

6.3 Required Test Equipment

The following test equipment will be required to calibrate the Model 1015.

1. Digital Voltmeter: DC range 0-100 volts, 3½ digit minimum.

2. Function generator: Output 20 volts, peak-to-peak. Frequency range .01 Hz to 1 MHz. Capable of sine triangle and square wave outputs.

3. X-Y Display or Oscilloscope.

4. Digital readout device as shown in Figure 6.15, page 59.

5. Y-DAC Alignment counter per Figure 6.16, page 59 Part #0115-0135

6. Oscilloscope Dual channel 50MHz Bandwidth.

It should be noted that the above list includes special test fixtures that will have to be constructed, or in the case of Item 5, ordered from the factory to perform a precise re-decalibration of the internal circuits. If this equipment is not available, recalibration of these circuits should not be attempted.

6.4 Power Supply

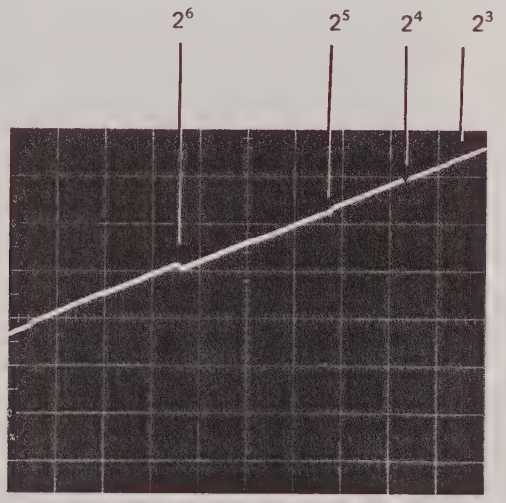
Place power supply regulator card on the extender card. Connect the negative lead of the Digital Volt Meter to the GND test point, which is a Cathode of CR-7. Note: See page 60 for location of test points and adjustment location. Connect

the positive lead of the Digital Volt Meter to the + 15 volt test point. Adjust the + 15 volt adjustment so the meter reads 15.00 volts. Connect the positive lead of the volt meter to the - 15 volt test point. Adjust the -15 volt adjustment until the output reads 15.00 volts. Connect the test lead of the volt meter to the +5 volt test point. Adjust the 5 volt adjustment pot until the output on the Digital Volt Meter reads 5.00 volts. Connect the test lead of the volt meter to the POWER ON test point. Adjust the power on the Potentiometer until the voltage on the volt meter reads 2.50 volts. Connect the test lead of the digital volt meter to the +15 test point. Adjust the line voltage to 130 volts. Adjust the high line shut down pot until the power supply drops to approximately 10 volts.

6.5 X DAC Alignment

Connect the vertical input of the Oscilloscope directly to the X output rear panel BNC. Trigger the scope externally on the Z-out from the 1015 rear panel. Set all input ground switches to the "GND"position. Arm and trigger the unit. Set display mode to Channel 1-4 verses time, horizontal expansion x 1. Set vertical gain of scope to .02 volts per division. Set horizontal time base to .1 Milli-seconds per division. Horizontal EXPANSION TO X 10. Adjust the DAC Pots in the following order: 2^3, 2^4, 2^5, 2^6, as shown in figure 6.3. See page 60 for location of adjustments.

Figure 6.3 CALIBRATE WAVEFORM



NOTE: Above Waveform has been misaligned to show location of transitions. Normal Waveform is a straight line.

Move the horizontal position of front panel and horizontal position on the scope for the 2^7 adjustment, 2^8, and the 2^9 posts.

6.6 Y DAC Alignment

Remove both memory boards from the unit, plug the Y-DAC counter alignment card part #0115-0135 into the ch.3, and 4 location. Connect the Y output from the 1015 to the vertical input of the oscilloscope. Trigger the scope externally on the Z output. Set the volts per division of the vertical amplifier of the scope to .02 volts. Set the horizontal time base to .1 milli-seconds per division and x 10 expansion. Adjust the vertical position control on the front panel of the 1015 and the horizontal position of the scope, until as shown in Figure 6.4.

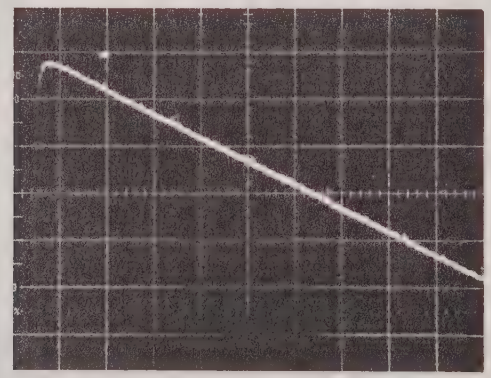


Figure 6.4 CALIBRATE WAVEFORM

Adjust the 2^5, 2^6, 2^7, 2^8 and 2^9 potentiometers (in that sequence). See page 60 for location of adjustments.

Adjust the Y output level so that the output is 1 volt, peak-to-peak. Reconnect display. Output should look like that shown in Figure 6.5

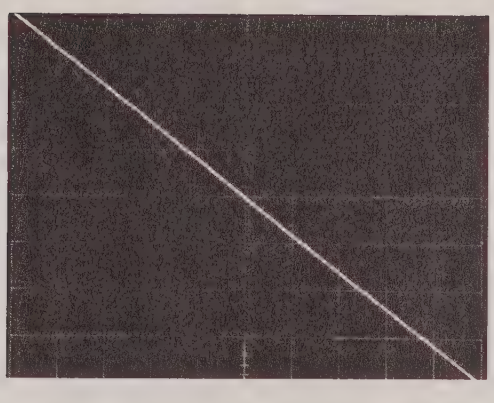


Figure 6.5 CALIBRATE WAVEFORM

6.7 Input Amplifier

Place the Channel 1 and 2 amplifier board on the extender card. Connect the vertical input of the oscilloscope to the 1st Amp test point. Set volts per division on the oscilloscope to .02 volts. Set scope trigger to "auto-mode". Set up front panel controls as follows:

Channels 1 through 4-volts full scale 50 ground all inputs, AC/DC coupling to the DC position, off set controls to midrange.

Rotate volts full scale control towards the .1 volt range. Observe base line on oscilloscope; this line should not move from the base line. If it does re-adjust "BAL" pot until no change occurs when rotating the control from the 50 VFS position to the .1 VFS position. Leave volts full scale selector in the .1 position. Set output of function generator to .1 volts. P-P, square wave, 1 KHz rate, connect output of function generator to Ch.1 input BNC. Trigger scope externally, on function generator sync output. Use insulated alignments. Adjust the 0.1 volt capacitor for the best square wave output. Figure 6.6 shows correct adjustment. Figures 6.7 and 6.8 show incorrect adjustment of compensation capacitor.

NOTE: These are typical on all ranges.

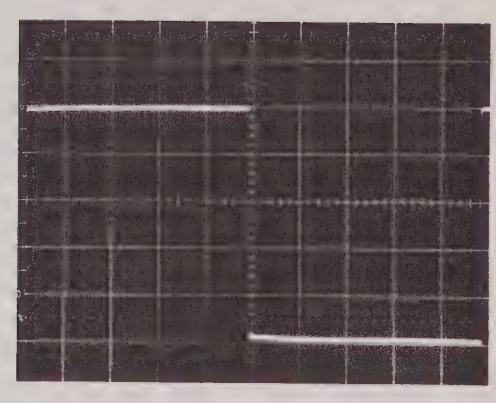


Figure 6.6 CORRECT WAVEFORM ADJUSTMENT

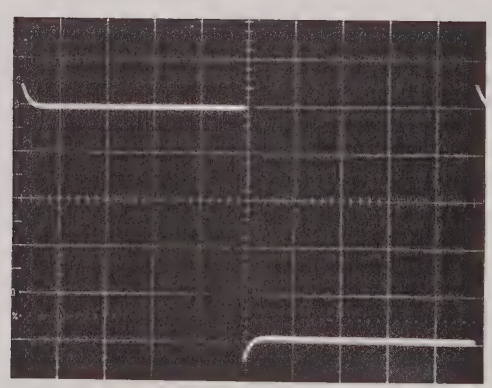


Figure 6.7 INCORRECT WAVEFORM ADJUSTMENT

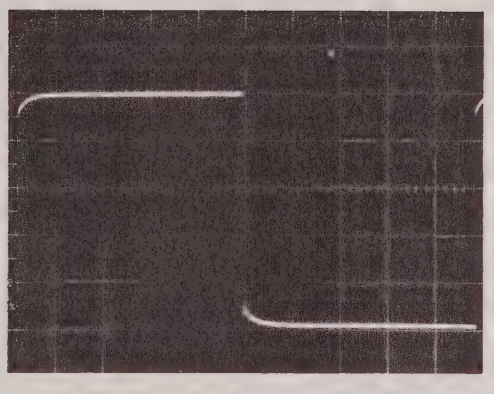


Figure 6.8 INCORRECT WAVEFORM ADJUSTMENT

Change volts full scale to 1 volt. Change output of function generator to 1 volt peak-to-peak. Adjust 1 volt range capacitor for best square wave.

Change volts full scale to 10 volts. Change voltage output from function generator to 10 volts full scale and adjust 10 volt cap to best square wave.

Connect the Oscilloscope probe to the output amplifier test point. Set the scope to .2 volts per division. Check the overall rise time of the amplifier; it should be 14 micro-seconds 10 to 90 percent. AS shown in Figure 6.9

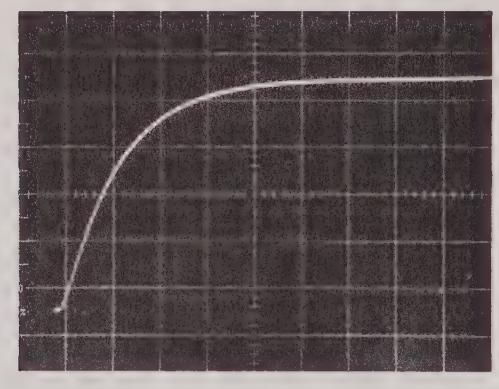


Figure 6.9 RESPONSE TIME MEASUREMENT

Repeat the above process for Channel 2, Channel 3 and Channel 4.

6.8 ADC Alignment

Place the counter multiplexer card corresponding to the ADC on the extender card. Input a 50 Hz triangle wave into Channel 1. Set level of function generator to exceed full scale by 10%. Set front panel controls as follows:

Input mode-channel 1-4 (1024).
Display mode-channel 1-4 VSt.
Turn all vertical outputs off except channel 1.
Adjust "INT OFFSET" pot for best output per figure 6.10.
see page 60 for location of adjustment.

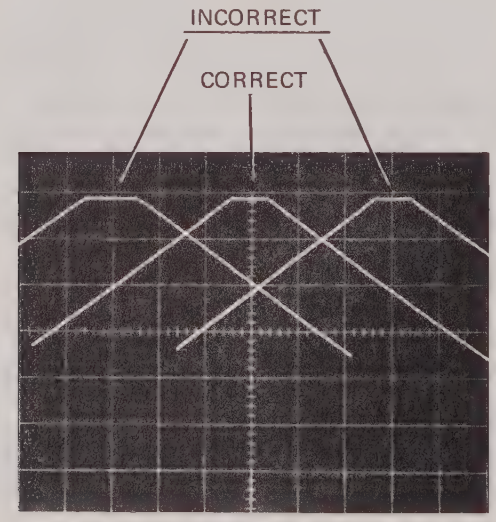


Figure 6.10 OFFSET POT ADJUSTMENT

Adjust the DLR pot for best output. Connect the vertical input of the Oscilloscope to counter multiplex card MC3, pin 2 -- for Channel 1 or 3. (MC6 pin 12 for Channel 2 and 4.) Set the trigger source on the scope to external. Externally trigger the scope on the trigger out BNC of the 1015. Input a triangle wave 1/10 of the full scale range.

Offset input to the top of the display. Trigger 1015 from Sync output of function generator, to Ext. input. (Negative slope.) Set scope sweep-time to 1Msec. Sweep mode to normal, positive slope. Use expansion of x 10 and center display on scope.

Adjust the "LIN" Pot for minimum "glitch" in the display and for best symmetry of the least significant bit on the scope. Figures 6.11 and 6.12 show the correct adjustment. Figures 6.13 and 6.14 show an incorrect adjustment of the "LIN" Potentiometer.

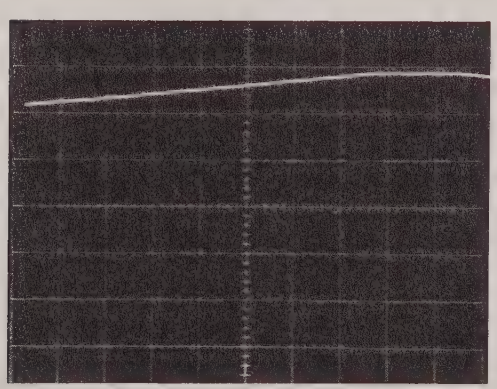


Figure 6.11 CORRECT LIN POT ADJUSTMENT

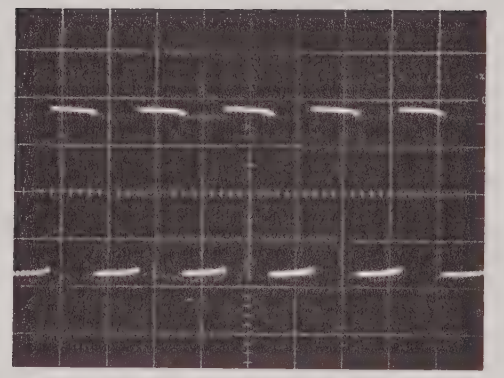


Figure 6.12 CORRECT LIN POT ADJUSTMENT

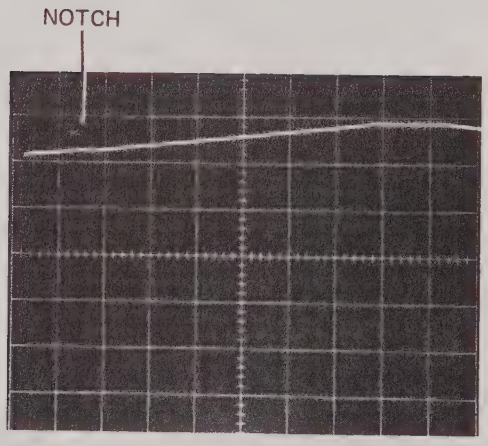


Figure 6.13 INCORRECT LIN POT ADJUSTMENT

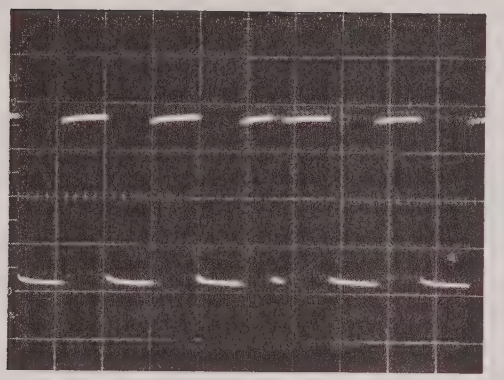


Figure 6.14 INCORRECT LIN ADJUSTMENT

Repeat the above steps for Channels 2 through 4, substituting these numbers for Channel 1 indication.

There are two methods described below to calibrate the scale factor of the analog to digital converter. The first method uses the special digital read-out device listed in Section 6.3. During factory calibration this digital method is used to provide a scale factor of 1000 counts in the converter for a full scale input. This allows a 23 word over scale factor before limiting occurs. When using the 1015 as a digital measuring device and high accuracy is required, the digital method must be used during re-calibration. However, if the 1015 is normally used only with an analog output device, such as a plotter or scope, the alternate (analog) method may be used.

6.9 Scale Factor Adjustment (Digital Method)

Using digital volt meter check the +5 on pin 14 of an integrated circuit on the counter multiplex board. Voltage must be 5.00 volts, if it is not, adjust the +5 adjustment on the power supply regulator card until it reads exactly 5.00 volts. Connect an X-1 scope probe to a 5 volt test point, on the counter multiplex card, and connect the BNC connector of the scope probe to the Channel 1 input. Ground all inputs. Set all volts full scale knobs to 5 volts full scale. Set all offset controls of all channels to minus (-) offscale. Turn

off all vertical outputs except Channel 1. Connect digital readout device to 50 pin rear panel connector. Set trigger until digital number on the digital readout device reads "1". Unground the input. Adjust "Scale Factor" potentiometer until digital readout device reads 1000. Lights 4, 3 and 0 should be OFF, ± 1 least significant bit. NOTE: After completing scale factor adjustment, return offset control to its full counter-clockwise position. There will be some interaction between the "offset" and "scale factor pots". Adjust the scale factor pot, to about half the number required each time.

Continue the above procedures for each input (Channel 2 through 4) - substituting these Channels for the Channel 1 references in the test procedure.

6.10 Scale Factor Adjustment (Alternate Method)

Set front panel controls as follows on Channels 1 through 4

Volts full scale - 5 volts

Offset - midrange

GND - Out (not grounded)

AD/DC - DC

Set function generator to 100 Hz square wave. Using a calibrated oscilloscope, adjust the output level to exactly 5.0 volts P-P. Connect this signal to the Channel 1 input. Place the Ch 1 & 2 ADC card on the extender board.

Connect the vertical input of the oscilloscope to the pin 6 of A3, Ch 1 and 3 (A4 for Channel 2 and 4).

Check the level; it should be 7.60 volts P-P. If it is not, readjust the scale factor control until it is.

Repeat the above for Channels 2 through 4.

This completes the calibration procedure. At this point you may want to perform the display calibration per Section 6.1 to provide a system calibration.

33

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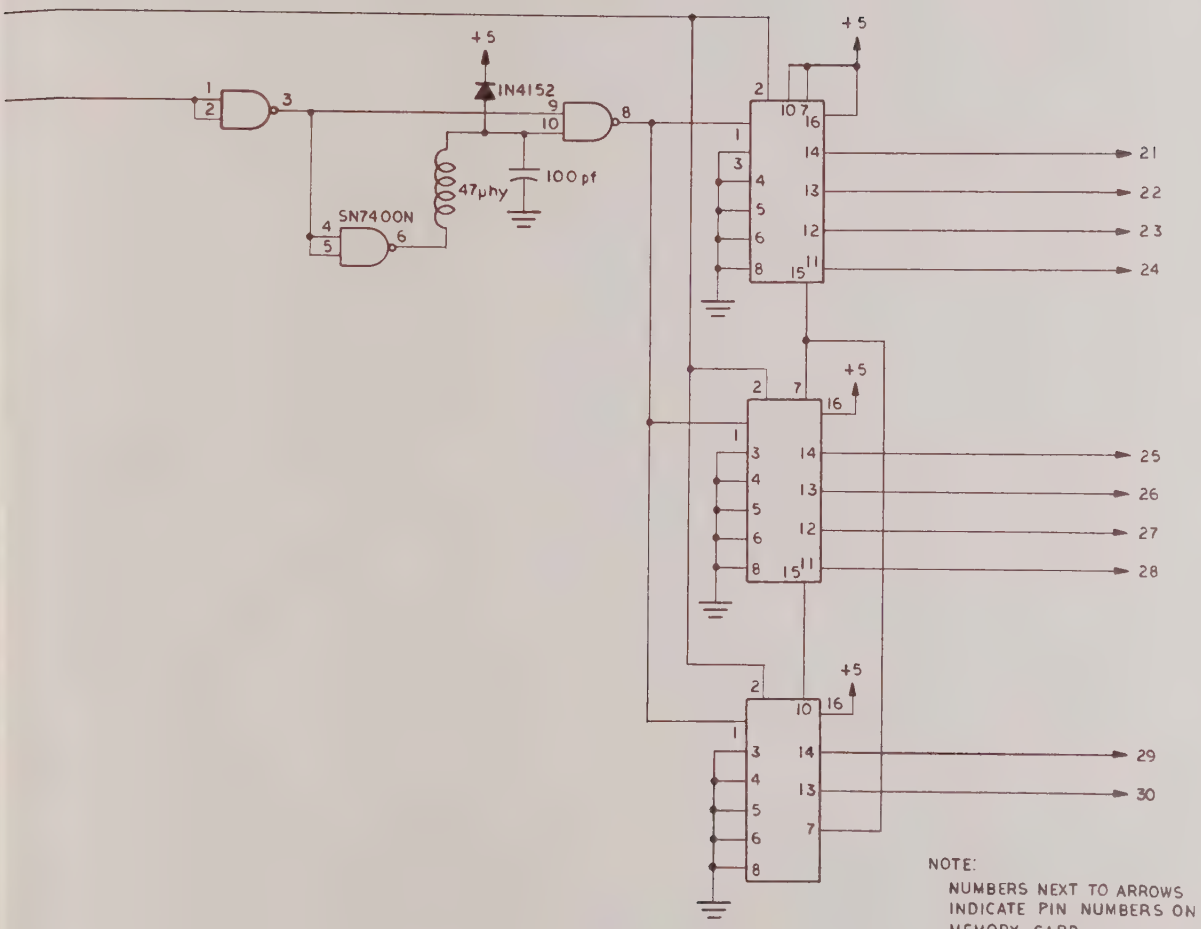
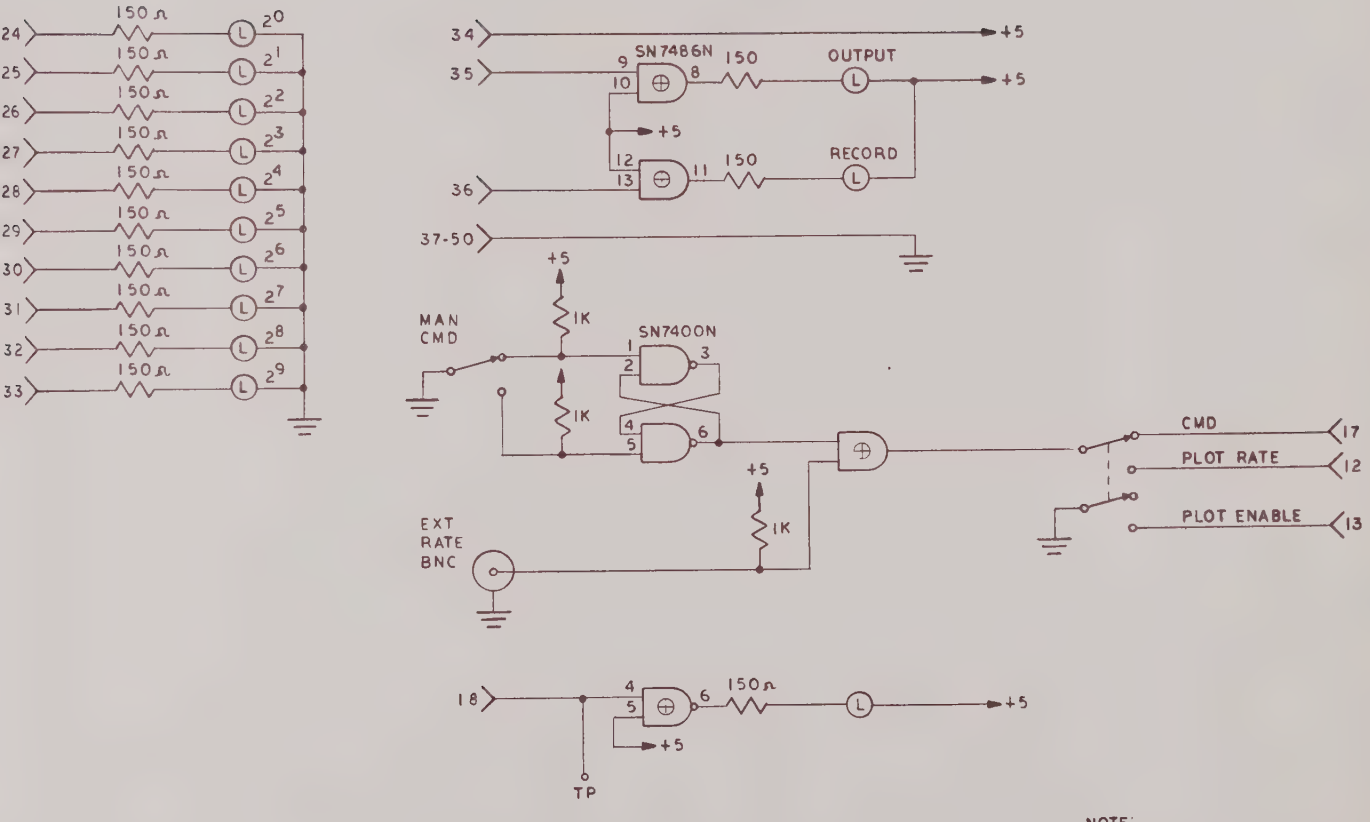


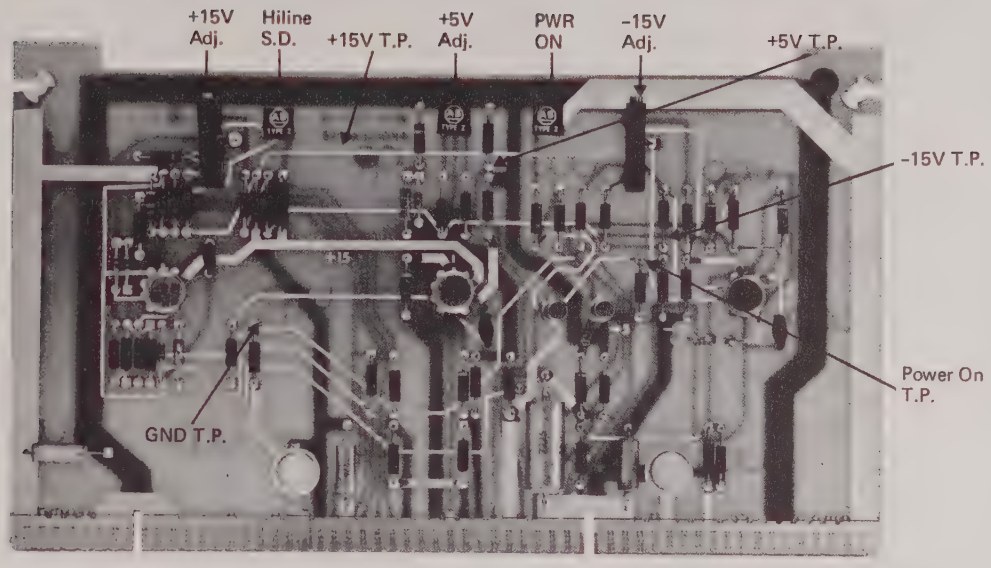
Y DAC ALIGNMENT TEST CARD



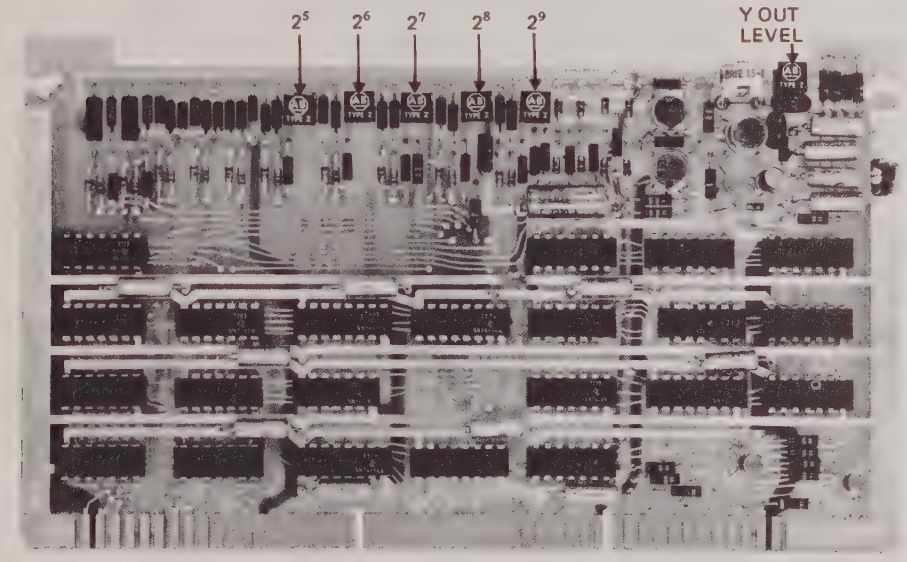
NOTE:
ALL LED'S ARE MONSANTO
NO MV5021 OR EQUIV.

1015 I/O TEST BOX

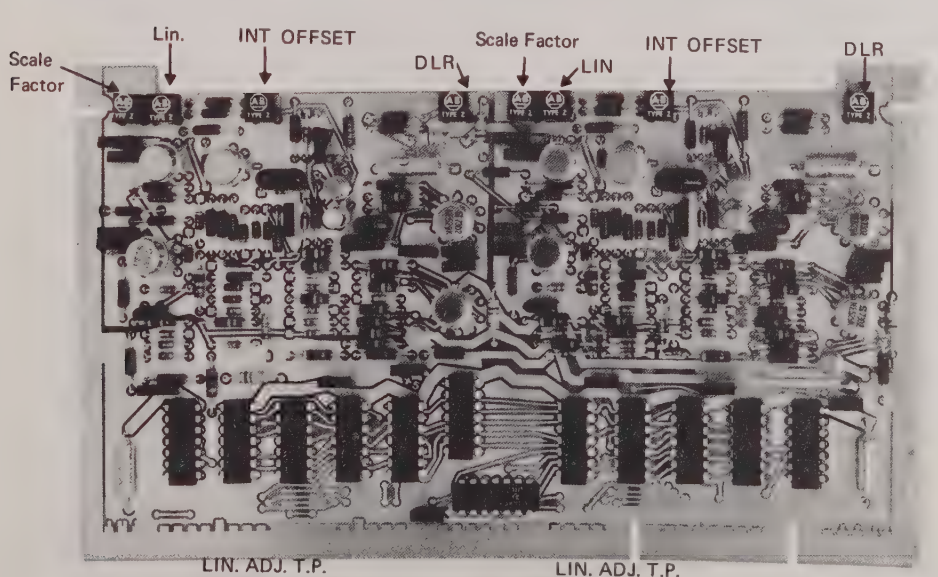
Alignment Test Card
and 1/0 Test Box



Power Supply Regulator Card



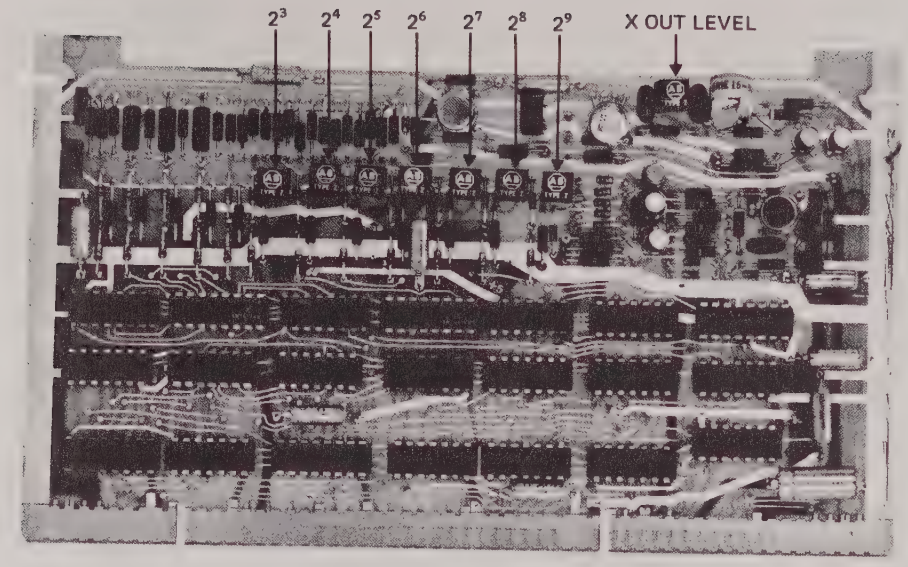
Y DAC CARD



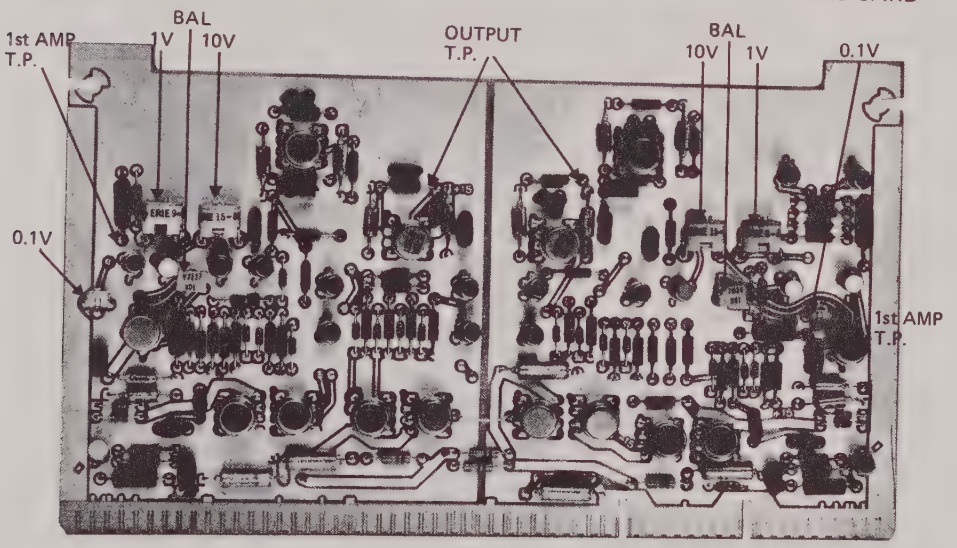
LIN. ADJ. T.P.
CONTR. MPX BRD
MC 3 PIN 2

LIN. ADJ. T.P.
CONTR. MPX BRD
MC 6 PIN 12

A/D Conv. Card



X DAC CARD



Input AMP Card

Test Point and Adjustment
Location Diagram

SECTION VII

7.0 Technical Description

This section presents the technical description of the Model 1015, and is intended to give service personnel an overview of the unit. This section is divided into two subsections: (1) Data Flow, and (2) Control Function. The block diagrams which accompany each subsection are foldout sheets located at the end of the appropriate subsection. For more detailed information, schematic diagrams are provided elsewhere in the manual.

7.1 Data Flow

Refer to Figure 7.1; 1015 DATA FLOW BLOCK DIAGRAM

7.11 Input Amplifier

Signals entering the input BNC connector flow through the AC/DC and grounding switches on the front panel, through the front panel/Motherboard connector to the Motherboard, and thence to the connector housing the appropriate input amplifier board. Each input amplifier board contains amplifiers for two channels.

The input amplifier consists of two inverting stages. The first stage utilizes an integrated circuit operational amplifier with field-effect input stage for its primary gain element. The voltage gain of this stage is switched in three decade steps from 0.1 to 10 by field effect transistors (FET) in the feedback loop, which are in turn controlled by decoded outputs from the appropriate "volts full scale" switch on the front panel. Diodes at the amplifier input terminal protect the amplifier from damage from input overloads. An FET source follower driven from the input terminal of the amplifier cancels the bandwidth-reducing effects of the parasitic capacitance of the gain-switching FET's.

The second stage is similar to the first, except that reduced impedence eliminates the necessity for either the source follower or the field effect input on the IC. The voltage gain of this stage is also switched by FET's in three ranges: 2,5, and 10, or selected by the decoded "volts full scale" switch. The FET switches vary the input resistance on this stage, rather than the feedback resistance because it is desired to keep a fixed feedback time constant.

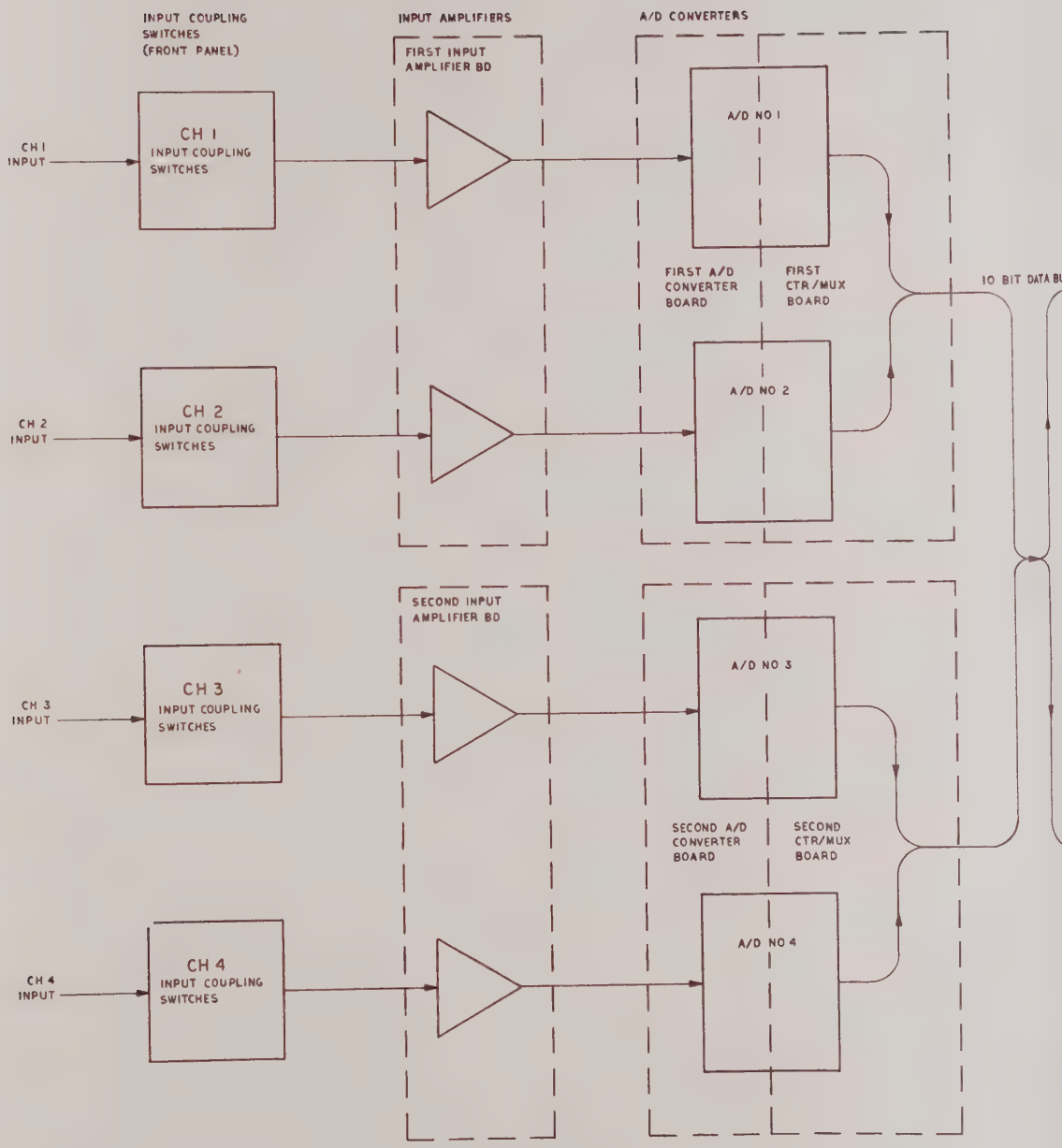
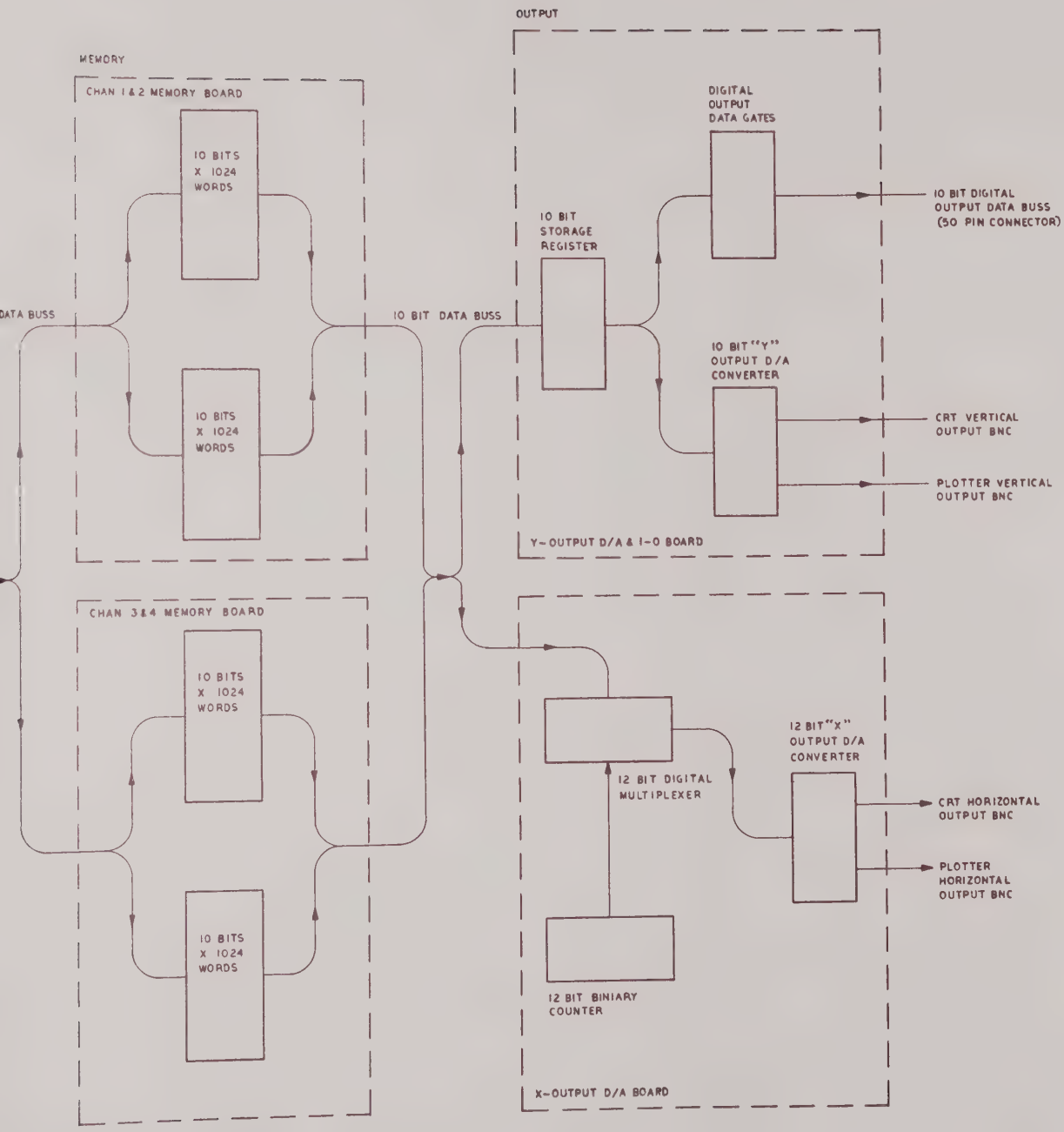


FIG. 7.1 1015 DATA FL



FLOW BLOCK DIAGRAM

Keeping a fixed second stage time constant gives the following desired effects:

(1) The effect on the amplifier output of the input offset control, which is resistively summed (after RC filtering and IC buffering), remains constant over the entire gain range. Additionally, the overall amplifier bandwidth can be controlled by the value, the feedback resistor and capacitor time constant.

(2) The overall amplifier gain can thus be switched in a 5,2, 1 sequence from 0.2 to 100, providing a constant 10V full scale output for full scale inputs ranging from 50V to 100MV, without disturbing amplifier bandwidth or zero offset position.

(3) The output of each of the four amplifiers connects to three places: (1) to the appropriate A/D converter inputs, (2) through a 10K resistor to the Trigger Source switch, and (3) to the inputs of the overrange comparators for that channel. The latter two terminations are on the front panel.

7.12 1015 A/D CONVERTER

The A/D. Converter used in the Model 1015 is a multi-slope type converter. This is basically a variation of the "dual slope" integrating type converter. With this in mind, it is useful to review the dual slope method of conversion and to examine its limitations and advantages.

A typical dual-slope converter block diagram is shown in Fig. 7.2

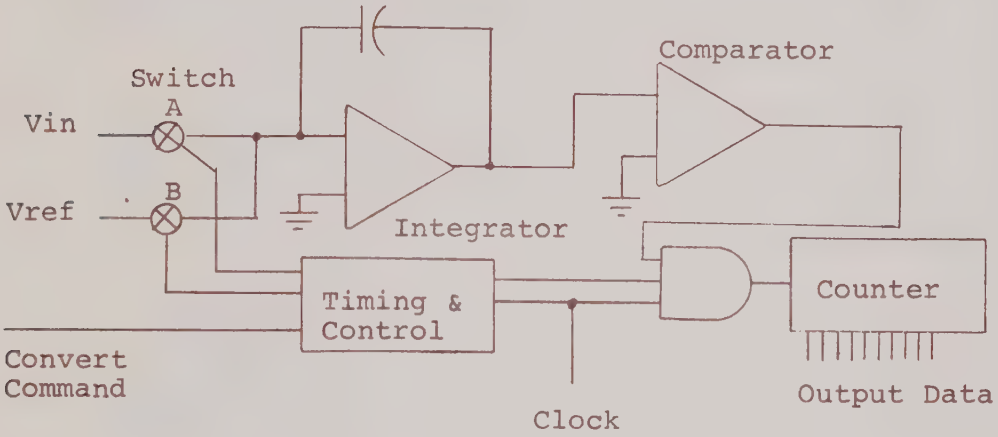


Figure 7.2 TYPICAL DUAL-SLOPE CONVERTER

The conversion period consists of two phases:

Phase 1 - Ingegration Period

During this period switch A is closed and switch B is open. The output of the integrator is a ramp with a slope proportional to the amplitude of the input signal. The integration period is determined by a counter in the timing and control logic which is driven from the system clock. The total time of the integration period is always determined by a fixed number of clock pulses; thus the output of the integrator at the end of the integration period is a voltage that is proportional to the input voltage and the clock period. (see waveform diagram, Fig. 7.3)

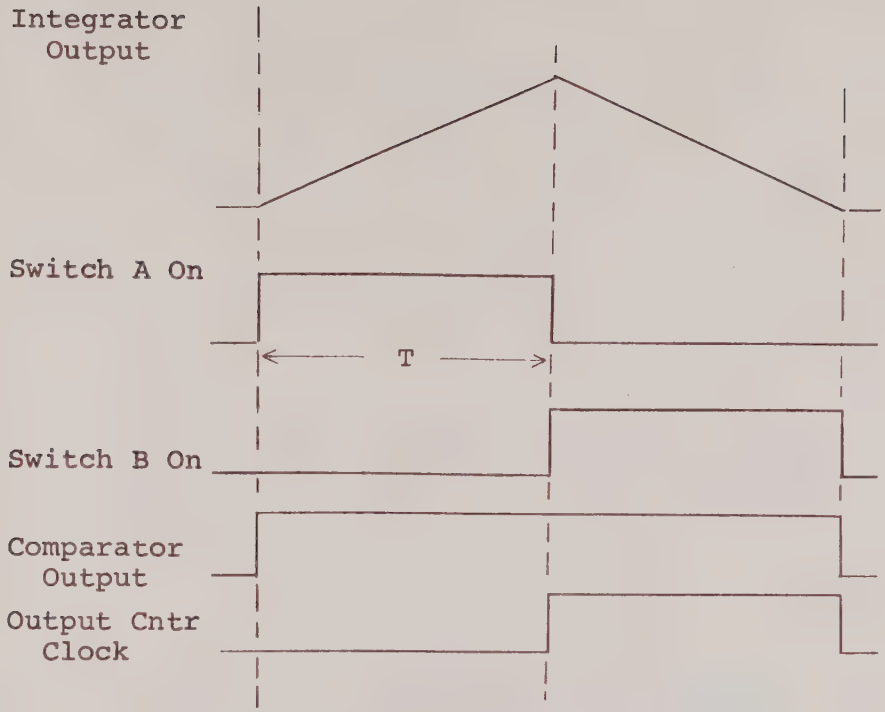


Figure 7.3 DUAL SLOPE WAVEFORM

This wave form is expressed by the following equation:

$$Vl = \frac{Nl\ Vin}{f}$$

N_1 = counts in integrate counter

K = integrator slope constant

F = clock frequency

Phase 2-Count period:

At the beginning of the count period, switch B is closed, switch A is opened, and the integrator output is a negative ramp starting at VI, with slope proportional to Yref. At the same time, clock pulses are gated into the output counter, which has been preset to zero. Vref is chosen to be V full scale. When the integrator output reaches zero, the counter and all switches are shut off, and the conversion is complete. The counter holds a number of counts proportional to the time it took this integration voltage to go from VI to ground. This is given by:

$$T = \frac{Vl}{K\ Vref} \qquad \text{since} \qquad Vl = \frac{Nl\ Vin\ K}{f};$$

$$T = \frac{Nl\ Vin\ K/f}{K\ Vref} = \frac{Nl\ Vin}{f\ Vref}$$

The number of clock pulses in the counter = $\frac{T}{1/f} = Nc$

substituting, we get $Nc = \frac{N1\ Vin}{Vref} \quad \frac{1}{1} = N1 \frac{Vin}{Vref}$

If N1 = 1024, and the output counter is 10 bits, we have a 10-bit A/D.

7.13 Advantages

Notice in the above equations that both the clock frequency and the integration time constant cancel in the final equation. This means that the clock and time constant are noncritical, as long as they do not change over one conversion period.

7.14 Disadvantages

Since the output counter is a 10-bit counter, 1024 clock pulses must enter it during the count period for a full scale input. Since this amounts to 1/2 of the conversion period, a full scale 10-bit conversion requires 2048 clock pulses. If the maximum conversion period is 10 μsec, as in the 1015, the clock period must be $10^5/2048$, which is less than 5 Nsec or a clock frequency of greater than 200 Mhz.

To utilize lower clock frequencies, a variation of the above circuits is used on the 1015. A block diagram is shown in Figure 7.4 and typical timing diagrams are shown in Fig. 7.5

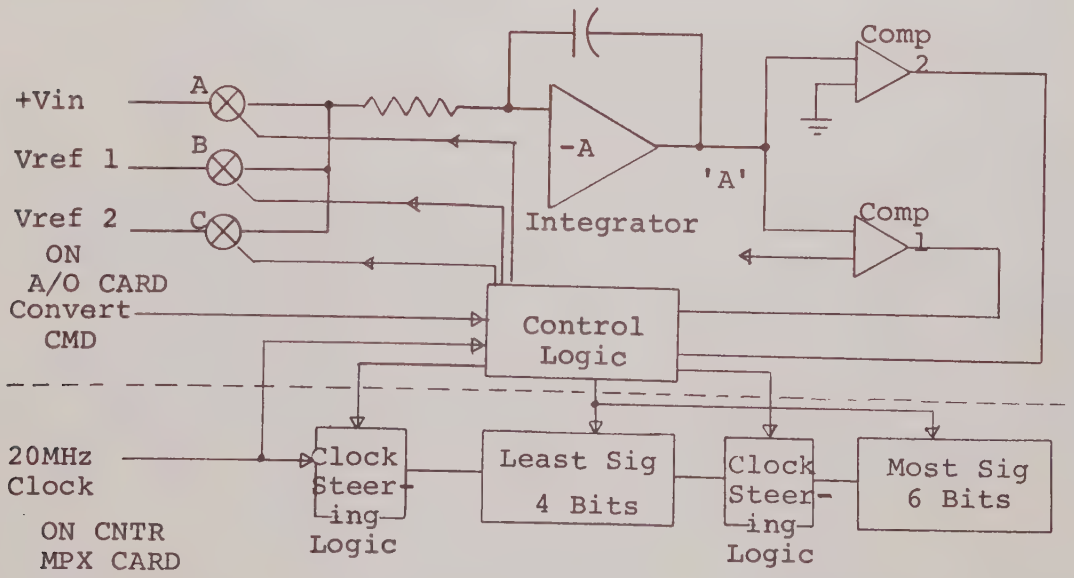


Figure 7.4 1015 BLOCK DIAGRAM

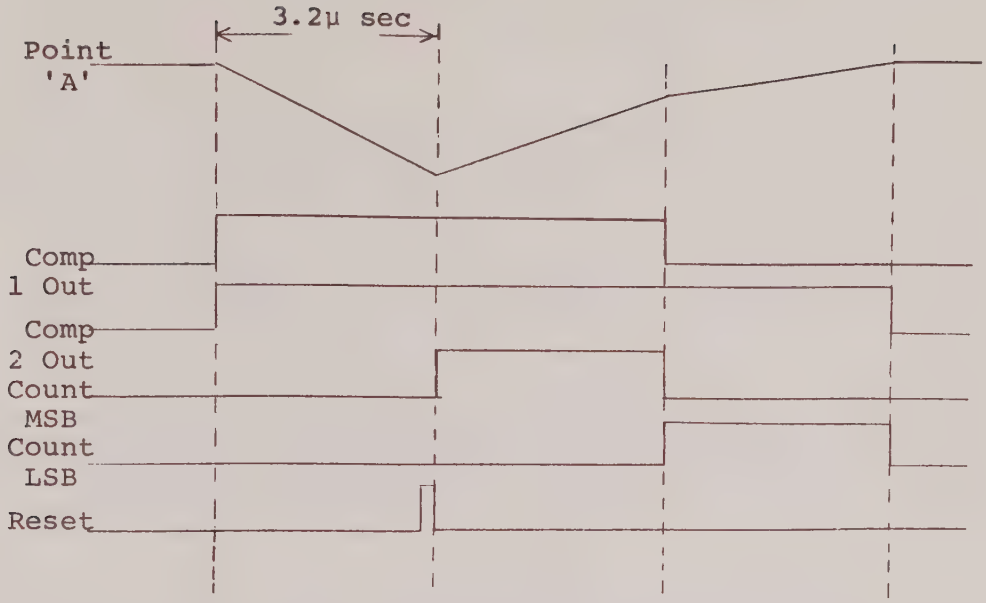


Figure 7.5 1015 TIMING DIAGRAM

The integration period is essentially the same as before, except that its time period is 32 counts of a 10 Mhz clock or 3.2 μsec. (This time interval is generated on the record control board). The count period however, is quite different. Note that there are two comparators, one biased at ground and a second biased at $-V_{thr}$, slightly below ground (the ramp on the 1015 A/D begins in a negative direction). Assume for the moment that the integrator voltage at the end of the integrate period is more negative than $-V_{thr}$. In this case then switch A is open, switch B is closed, switching $Vref_1$, into the integrator, and switch C remains open. At the same time, 20 Mhz is gated into the most significant six bits of the counter. $Vref_1$ and Vin are in such proportions that, if only the most significant 6 bits were used, a full scale "Vin" would result in 64 counts in the counter by the time the integrator reached zero volts. However, as the integrator output crosses $-V_{thr}$, a new count mode is initiated.

On the next clock pulse after comparator 1 switches, switch B opens and switch C closes, switching $Vref_2$ into the integrator. $Vref_2$ is adjusted to be exactly 1/16 of V_{ref1}. When $Vref_2$ is switched in successive counts of the 20 Mhz clock are gated into the least significant end of the 10 bit counter. Counting continues until comparator 2 switches, then all switches are opened. Counts will cease and the conversion is complete. This is the vernier count portion of the counter cycle, which gives the converter its 10-bit resolution.

Only two things are critical for accuracy; V_{ref1} and V_{ref2}. The location of the second comparator threshold is not critical although it must be a minimum voltage away from ground.

If Vin is very low, the integrator voltage at the end of the integrate period does not switch comparator 1 and the converter operates as a conventional dual-slope type converter using V_{ref2} as a reference.

A brief identification of the function of the components in the 1015 A/D converter follows. Refer to the A/D converter schematic diagram, #0115-0006. The components in the top A/D will be identified; the other A/D on the card is similarly drawn.

The input amplifier, A3, serves to precondition the input signal and temperature compensate it for the drift of the input switch diodes CR1 and CR15. R1 (scale factor) adjusts the overall gain of the converter. A1 and its components generate the two reference currents; I_{ref1} from pin 7 through R33, switched by CR11 and CR25, and I_{ref2} from pin 1 through R35, switched by CR13 and CR27. R3 adjusts I_{ref2} so that it is precisely 1/16 of I_{ref1}.

Q1, Q3 and Q5 make up the integrator amplifier; and C7 is the integrating capacitor. R11 adjusts integrator offset. Diodes CR7, CR17, and CR51 prevent the integrator from going overange too far, thus giving the A/D rapid overload recovery. A7 is the comparator that senses the switch point between the two reference currents, and comparator A5 senses the end of conversion. A feedback loop from A5 through R73, CR41, the diode network formed by CR31, 33, 35, 37 and R57 serve to keep the integrator output at the A5 comparator threshold between conversions. Thus the integration always begins from the same place.

The counter portion of the A/D converter is located on the Counter-Multiplexer card.

Signal TMH (see Section 10 for neumonic glossary) provides the 20 Mhz clock rate for the counter.

Flip flops MA4, MA2 and counter MB4 provide the 6 most significant bit counter and flip flops MA4, MA3 and MA2 and 4 the least significant counts. Signal RCA provides a reset command to the counter at the beginning of each conversion.

Signal EVA is the enable vernier count control. When EVA is low the upper section of the counter is enabled and when EVA

is high the whole counter is operational.

Signal ECA is the enable count command controlling when the counter advances. The outputs from the counter are fed back through a series of gates to prevent overflow of the counter.

The outputs of the counter are connected to the inputs of the DM8094 tri state logic gates. These gates are enabled in sequence by the record control logic. All of the outputs of the DM8094's are connected via a common 10-bit data bus to the memory inputs

7.15 Memory

Digital data from the A/D converters is connected to the memory by means of a 10-bit data bus on the Motherboard between the Counter 1/Multiplex cards and the Memory cards.

The 1015 memory contains 4096 10-bit digital words, partitioned into four separate memories containing 1024 10-bit words each. The memory is located on two identical PC cards, each containing a pair of 1024 word segments. Each memory segment consists of the following:

1. Input storage register

   Since the inputs are derived from a common bus, data inputs for each memory must arrive separately. However, the memories are for the most part clocked simultaneously, so there must be some intermediate "buffer storage" medium. The input storage register performs this function.

2. Memory elements

   Each memory segment contains 10 MOS 1024 bit dynamic "shift register" elements. These elements propogate data serially in 1024 steps from the input to the output, advancing the data one location for each clock pulse. The device thus "remembers" the last 1024 bits that entered its input. Memory of one 1024 bit sequence is achieved by connecting the output to the input and continuously clocking the device (data is lost if the clock frequency drops below a prescribed minimum). Data is written into the memory by momentarily connecting their inputs to the storage register outputs and clocking the memory once.

7.16 Output Gating

The output of each 1024 word memory segment is connected to a common data bus by means of "Tri-state" gates. The outputs of these gates behave like normal TTL gates when enabled, and revert to an open circuit when disabled; thus their outputs can be connected together.

7.17 Output Section

Output data leaves the 1015 in one of two forms: Digital or Analog.

7.18 Digital Output

Digital output data is generated on the Y output D/A & I-0 board. Digital data from the memory output arrives at the board via a 10-bit data bus, where it is stored in a 10-bit register. The register outputs are connected to a "Tri-state" output bus through polarity-determining exclusive-OR gates.

7.19 Analog Output

Analog outputs are provided on the 1015 so that visual representation of recorded data can be obtained if desired. The analog data is generated by two D/A converters (DAC), one for the horizontal (X) axis and one for the vertical (Y) axis.

The vertical output DAC and its 10-bit input register is located on the Y-output D/A & I-0 board. This DAC is the "current summing" type, the currents being switched by a diode pair for each bit. Current to voltage conversion is achieved by feedback around a differential amplifier and vertical expansion is achieved by switching feedback resistors with a FET switch. Vertical offset is selected by diode switch, depending on the channel currently being displayed. The offset control voltages are generated by one of the four output vertical position potentiometers on the front panel and are RC filtered and buffered on the Y - D/A & I0 board.

The output of the DAC amplifier is connected via resistive divider/noise filter networks to the display and plot Y output BNC connectors on the rear panels. An FET grounds the plot output when not in use.

The horizontal output DAC, located on the X-output D/A board, is similar to this Y D/A, except that its input register is preceded by a digital multiplexer. This allows the X D/A to select its input either from a binary counter located on the

board (to provide a ramp for Y-T displays) or from the memory output data bus (for X-Y displays). The resolution of the X D/A is 12 bits, because it must provide 4096 position sweeps when in the singoe channel Y-T output mode. The binary counter is altered by control logic to be a 10, 11 or 12 bit counter depending on the display mode. Expansion, positioning, and plot and display output distribution are achieved in essentially the same manner as on the Y D/A.

7.2 Control Logic

Refer to figure 7.6 1015 control logic block diagram.

The controls section of the 1015 can be separated into three main sections: Data input logic, display logic, and data output logic, with the time base affecting all three. There is some intervening of these functions, however, the sections are distinct enough to be described separately.

7.21 Data Input Control Logic

The bulk of this block is located on the Trigger Control, Record Control, and Memory Control boards. An additional portion resides on the Output Address board (Input Data and Memory Input Address Counter).

The Trigger and Control board is largely concerned with starting and terminating the record sequence, and switching the time base at the appropriate moment (if dual time base mode is selected). The trigger and delayed trigger flip-flops are on this board, as are the record and time base control flip-flops.

The Record Control board is concerned with the details of the record cycle. The logic on this board starts each conversion, controls the length of the A/D converter's integration period, addresses the data outputs of the converters and at the appropriate time strobes the data into the memory input registers and generates the write command signal.

The Memory Control board receives the write command signal from the Record Control board and distributes it to the four memory segments, as modified by the "Hold" logic located on the board. During single and dual channel input sequences, the distribution is also affected by signals from the input data and memory input address counter (located on the Output Address board), to give the effect of dual 2048 word or single

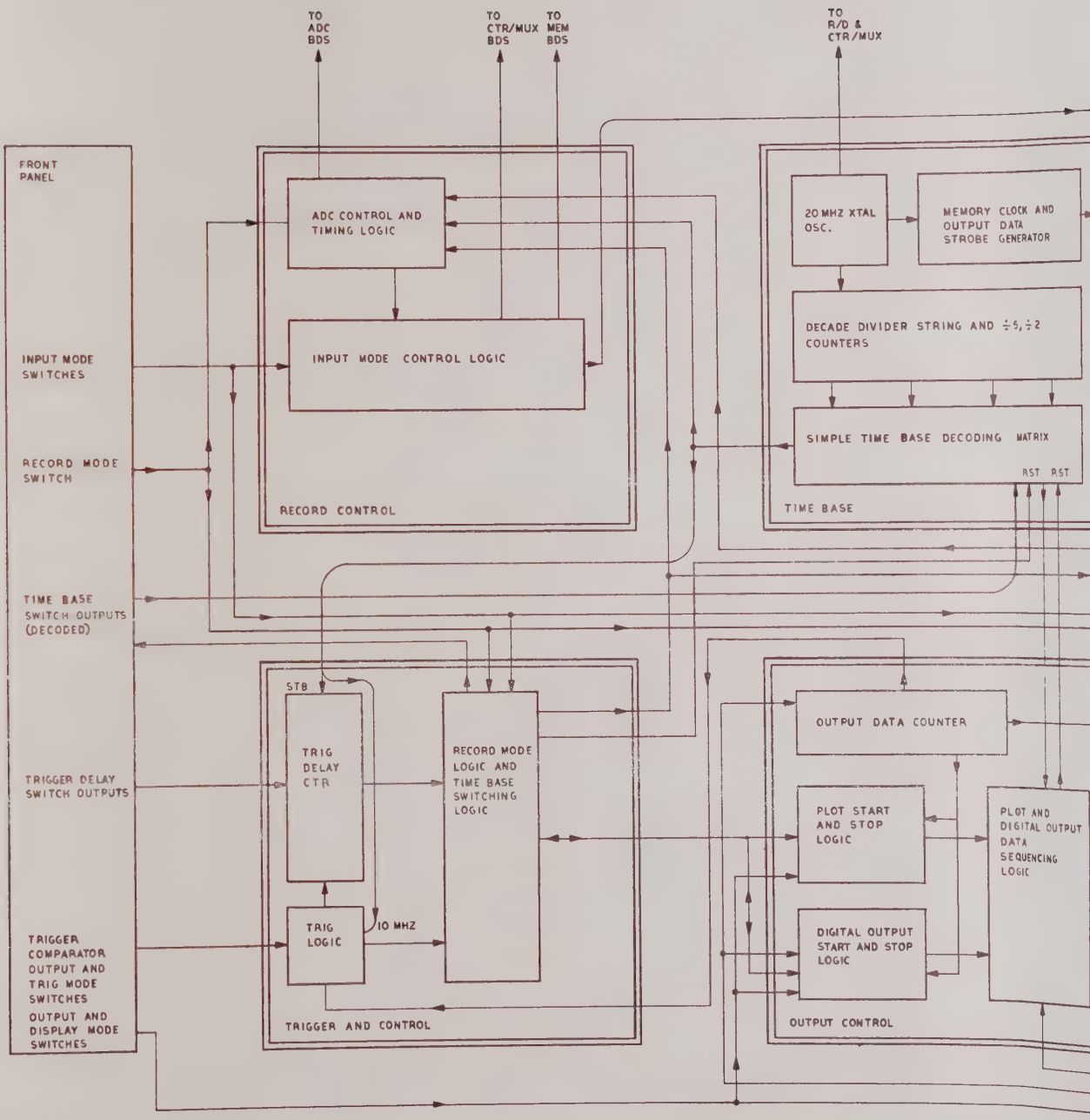
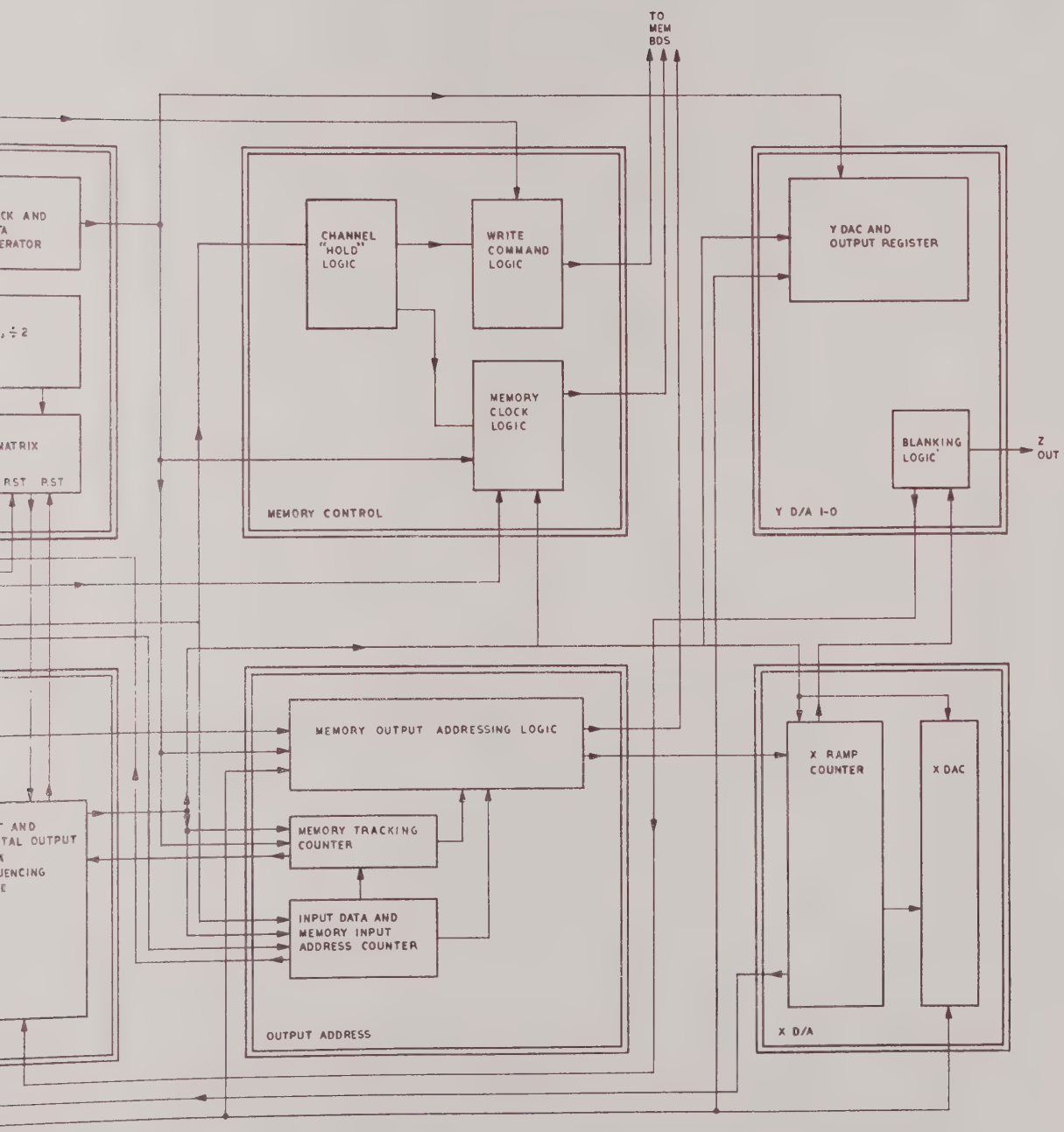


FIG. 7.6 1015 CONTROL LOGIC BLOCK



C BLOCK DIAGRAM

4096 word memories. During record sequences, the write command signal, from the Memory Control board, also controls the memory clock signals, again as modified by the "hold" logic. The clock distribution logic on this board is also controlled by the output logic when digital output and plot output modes are selected.

7.22 Display Logic

The CRT display controls are located on the output address board, the X-Output D/A board and the Y-Output D/A and I0 board.

7.23 Output Address Board

Output display mode switches connect to the Output Address board, where they are clocked into control flip-flops at the end of the current display cycle. The outputs of these flip-flops in turn control the memory addressing sequence for the CRT display and plot outputs, the X ramp generator count sequence and X-D/A input source, the Y-output D/A offset source switching, and the blanking and pen output sequence. The output memory address gates reside on the Output Address board. In display or plot mode, these gates receive their primary control from the display mode control flip-flops. In display mode, sequence timing information for these gates comes from the memory tracking counter (on the same board) and the output data counter, located on the output control board. This latter four-state counter advances once for every 1024 output words. The memory tracking counter advances once for each memory clock pulse; however, in display mode, it is present to the count left in the input data counter each time the output data counter overflows. This keeps track of the "origin" of the memory, especially after 2048 or 4096 word recordings in pretrigger mode, when the origin of the memory can be in either one of two or any of the four memory segments respectively.

7.24 X Output D/A

The X-ramp counter on the X-Output D/A board provides a binary X-sequenced drive for the X-Output D/A, thereby generating a ramp on the X-Output during Y-T display or plot outputs. Regardless of output mode, this counter advances one count for each Output Word. Timing for the end-of-sweep blanking is generated on this board by decoding the appropriate X-ramp counter states. Additional logic generates a pulse for every 1024 counts entered into this counter; this pulse drives the output data counter on the Output Control board.

7.25 Y-Output D/A and I-0 Board

The display control logic on this board consists of two small sections. The first is concerned with Y-D/A offset source control. This block derives control information from the output channel ON-OFF switches and the output mode control flip-flops and combines it with timing information from the output data counter to enable the appropriate Y-offset control for the channel being displayed.

The second section utilizes the same control and timing information, plus timing from the end-of-sweep blanking logic on the X-ramp counter, to derive the Z and $\overline{Z}$ output signals to blank the oscilloscope during retrace and undesired channel display.

7.3 Data Output Logic

The primary section of the data output logic is located on the Output Control board; signals from this board can be divided into two sections: Initiation and termination logic consists of one flip-flop each for plot and digital output modes, plus additional gating to sense the appropriate conditions for setting and resetting these flip-flops. The control signals for this gating come from front panel or rear connector commands, and timing is derived from X-ramp counter overflows (digital start) and from output data counter overflows (digital stop and Plot start and stop).

The plot and digital modes share the same data sequence and timing logic. This logic controls the memory clock and output register strober in response to commands from the word command line (in digital mode) and the internal or external plot time base line (in plot mode) as modified by delay pulses from the time base and overflow signals from the memory tracking counter.

Logic on this board also utilizes blanking signals from the Y-Output D/A and I-0 board in plot mode to generate the pen control output and plot output ungrounding signals and to skip (by "hurrying" through at display rates) undesired channels.

7.31 Output Address Board

This board performs essentially the same function as in display mode. However, the input data counter supplants the memory tracking counter as an address and timing source, and in digital output mode only, control signals for address sequencing are taken from flip-flops whose states reflect the input mode used in the last record cycle. The memory tracking

counter serves to flag the location in the memory of the next word to be output whenever the output intervals are so long as to require memory refresh cycles.

7.32 Memory Control Board

Signals from the Output Control board cause the logic on this board to generate appropriate clock signals during data advance and memory refresh cycles.

7.33 X-Output D/A Board

Overflow signals from the X-ramp counter on this board determine the digital output start time and advance the Output Data counter.

7.34 Y Output & I-O Board

This board contains the digital output register and data bus and the device address decode logic for the output status and command signals to and from the rear connector.

7.35 Time Base

The time base board contains a 20 MHz crystal oscillator which drives two counter chains; one that generates the memory clock, and another that generates the input sample time base by means of a decoding matrix controlled by the front panel time base controls. Other signals generated by the second count chain is used in various places in the instrument.

SECTION VIII

8.0 Maintenance

This section covers maintenance and disassembly procedures for trouble-shooting and repair of the Model 1015. Trouble-shooting is performed with the aid of a diagnostic procedure for the front panel controls and functions. This procedure provides sufficient detail to isolate a problem to the circuit board or module level.

A PC board exchange program has been set up with the factory for use by customers within the continental United States, and with regional service centers in foreign countries. In addition, waveform photographs have been included with the schematics to aid service personnel who wish to trouble-shoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800 TWX 910 338-0509.

In summary, there are three methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Trace the problem to the defective PC board and obtain a replacement board from the factory, or service center.

3. Trouble-shoot the problem to the component level with the aid of the diagnostic procedure and schematics or with the aid of factory personnel.

8.1 Diagnostic Procedure

The following test equipment will be required to conduct the diagnostic procedure:

1. A function generator capable of sine, triangle and square wave function over the frequency range of .01 Hz to 1 MHz and with a variable output of up to 20 volts peak-to-peak into a 250K ohm load, (four 1 meg ohm loads in parallel).

2. An oscilloscope: 2 channel DC to 50 MHz input bandwidth.

If a display device is not normally used with the Model 1015, an additional oscilloscope or CRT display will be required during the testing period. This latter oscilloscope need only have a 2 MHz input band width.

Connect the display device to the 1015 per figure 4.3, page 32. Turn on the equipment and allow them to stabilize for approximately 10 minutes. Before beginning the diagnostic procedure, the maintenance technician should read Section 3 through 6 of this manual. Note: All Section VIII figures are on the fold-out, page 88 .

Diagnostic Procedure	Trouble-Shooting Procedure
Set up front panel controls as follows:	
Channel 1 - 20 volts full scale, offset to mid-range	
Record/Hold - Record	
Ground button - Out	
AC/DC - DC	
Channel 2 - same as Channel 1	
Channel 3 - same as Channel 1	
Channel 4 - same as Channel 1	
Record Mode - Delayed	
Input Mode - Channel 1-4 (1024)	
Trigger group - Delay 0.00	
Source - Channel 1	
Mode - Single	
Coupling - DC	
Slope - Positive	
Trigger Level - mid-range	
Time base - Sample interval A-.01 M sec. A only mode	
Display horz. x 1 horz. position approx. mid-range	
Vertical expansion x 1 - all display Channel 1-4 should be on display mode Channel 1-4 VSt	
Output mode - Off	

Diagnostic Procedure	Trouble-Shooting Procedure
Connect function generator output to the input of the 1015 as shown in figure 8.1. Set output rate of function generator to 100Hz Triangle wave 20V P-P. Arm Unit. Output should look like figure 8.2, some adjustment of the vertical position controls may be necessary to get the traces to line up as shown in figure 8.2.	
	No display on output device, check all connections between 1015 and the output device. Check the power supply voltages, in the Model 1015. Recheck front panel controls per set up procedure. Check waveforms 1,2,3 and 4 on the time base board. Check the trigger and Control board for proper status of chip B6 pin 8, this pin should be high. Check waveforms 1,2,3 on the Y output D/A - I/O board. Check waveforms 1,2,3 and 4 on the X output D/A board. If only one or two of the triangle waveforms shown in figure 2 are straight lines, check the front panel controls, input amplifier A to D converter, counter multiplexer and memory for the effected Channels.
In the x 1 position the hortizontal output should be full scale on the display. Change the display mode as follows: Vertical expansion x 4, adjust one of the Channels, to the center of the display. Observe the waveform very carefully, make sure there are no gaps or glitches in the data. Also check the output level should be full scale on the display.	
Input Amp and ADC	
Return the vertical expansion to the x 1, re-adjust the Channel 3 vertical position for proper alignment per figure 8.2. Set the output function of the function generator to a square wave, frequency 10 Hz. Change sample interval rate to .1 M sec. Change sample interval rate to .1 M sec. Change the Channel 1 input	

Diagnostic Procedure	Trouble-Shooting Procedure
coupling switch to the AC position, Channel 4 to the AC position. Arm unit. Output should look like that shown in figure 8.3.	
	Check operation of front panel switches.
Ground all inputs, arm and trigger unit display should be four straight lines. Return the ground switches to their out positions on all Channels. Change the AC/DC switches to their DC positions. Change output function to sine wave on function generator. Arm Unit. Output should be as shown in figure 8.4. Place the Record/Hold switches to Hold positions, on Channel 1,2,3 and 4. Change the function of the function generator to a triangle waveform. Arm Unit. Output should still look like figure 8.4.	
	Check for proper operation of memory control card.
Release the Record/Hold switches. Arm unit, output should look like figure 8.2. Change front panel controls to as follows: Sample interval .01 M sec. Set trigger mode to Normal. Set output rate of function generator to 100 Hz. Unit should continuously arm and trigger.	
	Check trigger and Control board.
Rotate offset controls through their entire range. Check to make sure that the offset lights work in both the positive and negative directions so that all but about 40% of the signal is off scale.	
	Check offset controls on front panel outputs and check for proper operation of offset amplifier on input Amplifier boards.
Set the volts full scale control to the 50 volts peak to peak. Display should be as shown in figure 8.2 (full scale). Readjust the input offset controls so that the signals are symetrical around zero.	

Diagnostic Procedure	Trouble-Shooting Procedure
Change the volts full scale to the 10 volts position on all four Channels. Change the function generator output to 10 volts P-P. OUtput should be as the same as figure 8.2. Change the volts full scale to the 5 volts position Channel 1 thru 4. Change the output of the function generator to 5 volts peak to peak. Output should be as shown in figure 8.2. Continue this procedure until all input ranges have been checked.	If any of the volts full scale positions do not operate, check the volts full scale logic on the front panel and check the input amplifier per the input range truth table for proper operation.
Return volts full scale controls to the 10 volt position on all four Channels. Return the output of the function generator to the 10 volts P-P output. Check the ADC alignment on each output Channel by setting the vertical expansion to x 4. Examine each output, check for monotonic changes in data.	If data is not monotonic or there are glitches in the data check the analog to digital converter for proper alignment, (see section 6.8) for procedure. Check counter multiplex card for proper operation and check Memory boards for correct data output, waveforms 4 thru 13.
Input/Display Mode	
Change the front panel controls as follows: Set trigger mode to single input mode to Channel 1 (4096) Display mode to Channel 1 VSt (4096) Arm Unit.	If either the input mode or the display mode fails to operate properly, check for proper operation of the Record Control board and the Memory Control board and the output address card.

Output should be as shown in
figure 8.6
Change input mode to Channel 1
and 2 (2048)
Display mode to Channel 1 and 2 VSt
Arm Unit.
Output should be as shown in figure 8.7
Change front panel controls as follows:
Input Mode to Channel 1-4 (1024)
Display mode to Channel-4 VSt
Arm Unit.
Output should be as shown in figure 8.2
Change front panel controls as follows:
Channel 2 input to ground
Channel 3 input to ground
Channel 4 input to ground.
Display mode-Channel 1 VSt (4096)
Arm unit.

Output should be as shown in figure 8.8
Change front panel controls as follows:
Input mode - Channel 1 Mem 2 (1024)
Change function generator to sine wave
output.
Arm unit.
Output should be as shown in figure 8.9
Change front panel controls as follows:
Input mode - Channel 1 mem 3 (1024)
Change function generator output to a
square wave.
Arm unit.
Output should be as shown in figure 8.10
Change front panel controls as follows:
Channel 1 mem 4 (1024)
Change output of function generator to a
triangle wave
Arm unit.
Output should be as shown in figure 8.11
Change front panel controls as follows:
Input mode - Channel 1 - 4 (1024)
Output of function generator should be a
sine wave.
Arm Unit.
Change front panel controls as follows:
Channel 1 Record/Hold to Hold and un-
ground Channels 2,3, & 4. Change time
base sample interval A to .02 M sec.
Arm unit.
Change front panel controls as follows:
Display mode - Channel 2-4 vs Channel 1
Output should be as shown in figure 8.12
This checks the X-Y output mode of
operation.

Diagnostic Procedure

Trouble-Shooting Procedure

If the X-Y output mode fails to operate check the output address card for proper operation, also check the X DA converter.

Change front panel controls as follows:
Channel 1 Record/Hold to Record
Display mode - Channel 1-4 VSt.
Sample interval - .01 Msec.
Trigger mode to normal
Advance the digits on delay control. As this control is advance the output waveform should appear to move to the left.
Change the record mode form delayed to pretrigger. The front half of the output should appear to be discontinous. Advance the delay control to about .40 a continous sine wave should be present on the output.

Trigger & Arm

Change front panel controls as follows:
Delay 0.00
Record mode to delayed.
Display mode vertical exp. x 4
Turn all channels off except Channel 1
Center Channel 1 in the middle of the display.
Change the output of the function generator, to a triangle waveform.
Set the frequency to 50 Hz.
Adjust the triggering level so that exactly 1/2 cycle is present on the output display as shown in figure 8.13.
Advance the 100th's digit of the delay control one digit at a time, with each advance the waveform should appear to move to the left by 1/10th of one division on the display.

If the delay does not work properly, check the delay counter located on the trigger & Control board for proper operation.

Return the 100th's digit to the zero position. Advance the 10th's digit, with each advance of this digit the waveform should appear to move to the left, one major division.
Return the 10th's digit to the zero position.

Diagnostic Procedure	Trouble-Shooting Procedure
Advance the units digit one digit at a time with each advance the waveform should appear to invert on the odd numbered digits and be right side up on the even numbered digits. Return the delay control to the zero position. Change front panel controls as follows: Turn the Channels 2,3 and 4 outputs to the On position. Change the vertical expansion back to x 1. Change output rate of function generator to 100 Hz. Re-center the output waveforms if necessary.	
Trigger Source	
Per the original front panel set-up the trigger source should be Channel 1, if it is not, place the trigger source to the Channel 1 position. To verify that Channel 1 is triggering the instrument, ground the input of Channel 1 if triggering stops and the trigger ready light comes on, this indicates that the trigger source was Channel 1. Continue this procedure for Channel 2 source position, Channel 3 source position.	
	Trigger source fails to function properly check the front panel circuits and the trigger coupling circuits on the front panel.
Change the trigger source to external. Press the "manual" button on the front panel this should trigger the instrument each time that it is pressed. Reconnect the signal cable that is presently connected to input 4 to the external trigger input. The unit should begin triggering continously form this signal.	
Trigger Mode	
Change trigger mode to auto. In the "auto" mode the instrument should trigger by itself, without any aid from the external or internal trigger.	

Diagnostic Procedure

Trouble-Shooting Procedure

If any of the trigger modes fails to operate properly, check for proper operation of the triggering control circuit board.

Change the trigger mode to "normal"
Trigger should be derived from the signal or from the external source.
Unit should arm and trigger continously. Place the trigger mode to the "single" position. Manually arm the unit with the front panel "arm" push button.
Change front panel controls as follows:
Trigger mode - normal
Trigger source - Channel 1
Sample interval - .1 Msec. A only
Change the output rate of the function generator to 1Hz.
Change the trigger coupling switch form the DC to AC position.
Change the vertical expand to x 4 position.
Observe the output waveform as the switch is moved in and out. The triggering should become more negative on the slope when the AC position is selected. Change the slope position form positive to the negative.
The output should appear to invert.
Re-align the display Channels on the output display.
Return the sampling interval to 100 Hz.
Rotate the trigger level control through its range. Full range of the trigger level control should be from the very positive extreme of the waveform to the very negative extreme of the waveform.

Time Base

Change front panel controls as follows:
Turn off All vertical outputs except Channel 1
Center Channel 1 on the display
Adjust the trigger level controls so that one full cycle is visible on the display.
Set the sample interval control per table 1:

TABLE I

Function generator frequency	Sample Interval	#OF cycles on output
100 Hz	.01 Ms.	1
100 Hz	.02 Ms.	2
100 Hz	.05 Ms.	5
10 Hz	.1 Ms.	1
10 Hz	.2 Ms.	2
10 Hz	.5 Ms.	5
1 Hz	1 Ms.	1
1 Hz	2 Ms.	2
1 Hz	5 Ms.	5
.1 Hz	10 Ms.	1
.1 Hz	.01 Ms.	1

Note: .02 sec - 10 sec. check by clock

Diagnostic Procedure

Change front panel controls as follows:
Sample interval A - .01 Ms
Sample interval B - .01 Ms
Time base mode - Dual
Check sample interval B by changing sample interval B control per Table 1 Note: Leave sample interval A at .01 Ms position.
Change front panel controls as follows:
Time base sample interval A to 1 Msec.
Sample interval B to 2 Msec.
Mode - dual time base
Set trigger delay to 0.50
Set trigger mode to single
Set output frequency of function generator to 1 Hz.
Arm unit output should be as shown in figure 8.14.
Change record mode to pre-trigger.
Arm unit.
some discontinuinity could appear in the first half of the waveform. This test also verifies that the unit will operate across the interlace barrier.

Trouble-Shooting Procedure

If any of the time base sample interval rates, do not function properly check the decoding logic on the front panel, and also the time base card for proper operation.

Diagnostic Procedure

Trouble-Shooting Procedure

Set sample interval A control to .01 Msec.
Set the output of the function generator to 1000 Hz.
Arm unit.
10 cycles should be visible on the output display.
Change the Horz expansion to x 2, 5 cycles should be visible on the display.
Change the Horz. expansion to x 5, 2 cycles should be visible on the display.
Change the Horz. expansion to x 10, 1 cycle should be visible on the display, vert. mode.
Set the vertical expansion to x 1.
Set the On/Off switches on all four Channels to the On position.
Set the horz. display back to x 1.
Change the output rate of the function generator to 100 Hz.
Reconnect the signal to the Channel 4 input.
Arm unit.
Output should appear as it did in figure 8.2.
Individually turn each Channel on and off to verify that the On/Off switches for each Channel work properly.

Output Mode

Connect the "digital readout device" to the rear panel connector, connect the CMD input to the TB output BNC. Set the output mode to the "auto digital" mode, readout device. Place the trigger mode to the "normal" position. Unit should now continously arm and trigger output data.

If any of the output modes fail to operate properly check the front panel decode logic and the output control board for the proper operation.

With an oscilloscope check to make sure that the flags occur at a 10 Msec. rate at the flag test tack on the read-out device, flickering should be visible in the display.

Diagnostic Procedure	Trouble-Shooting Procedure
Display should be visible only once in a while. Flags should occur at a 10 Msec rate.	
Change front panel controls as follows:	
Trigger mode - Single	
Output mode - Off	
Now change the output mode to "edit".	
Arm unit.	
Sample interval to 10 Msec.	
Press the "digital" button. All Channels should disappear from the screen.	
Digital output numbers should increase to full scale value and then decrease to zero at a binary rate.	
The "output" light on the digital read-out device should be on.	
With the output mode still in the "edit" position press the "plot" push-button.	
The plot mode should begin at its internal rate.	
Change the digital readout device "output-plot" switch to the "plot" position.	
The PEN light should come on while unit is in plot.	
The display should sequence through Channel 1 through 4, in that order.	
Press the "plot" push-button again.	
With an oscilloscope check to make sure that the analog outputs are present, at the "X-plot" BNC connector on the rear panel. At the end of the plot, check to make sure that these outputs return to ground.	

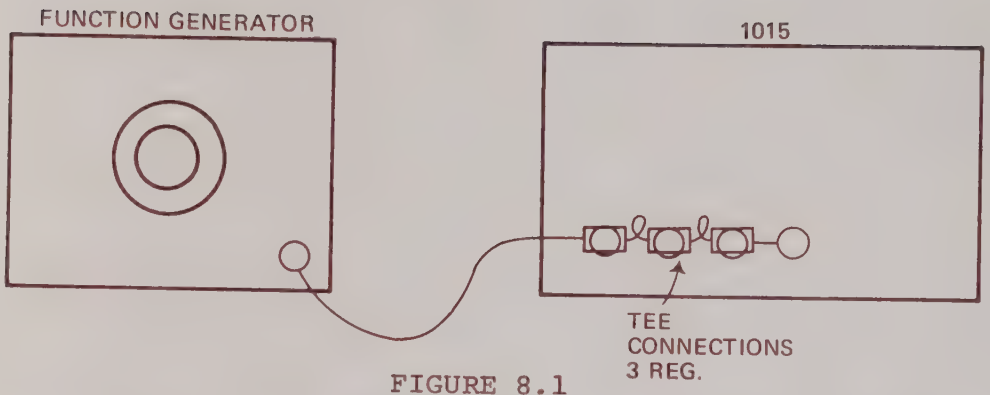


FIGURE 8.1

FIGURE 8.4

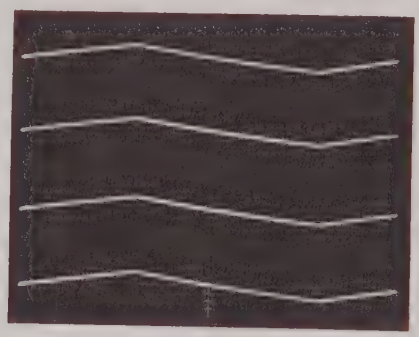


FIGURE 8.5

FIGURE 8.8

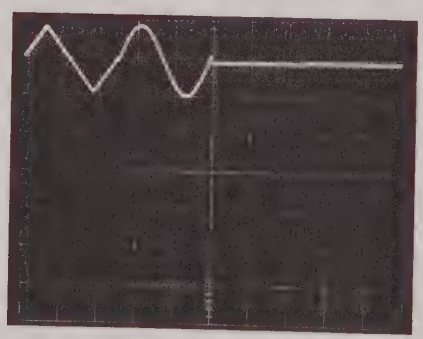


FIGURE 8.9

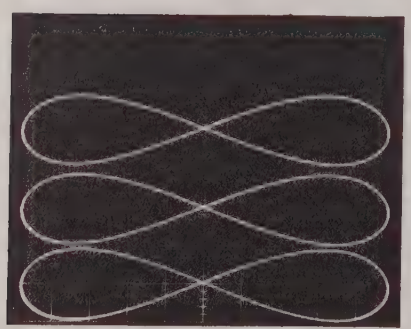


FIGURE 8.12

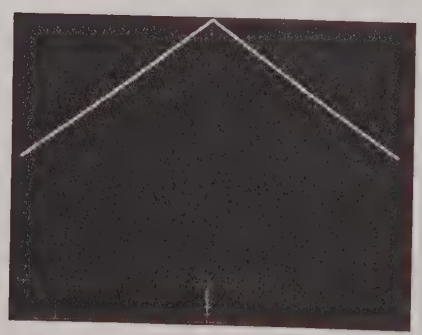
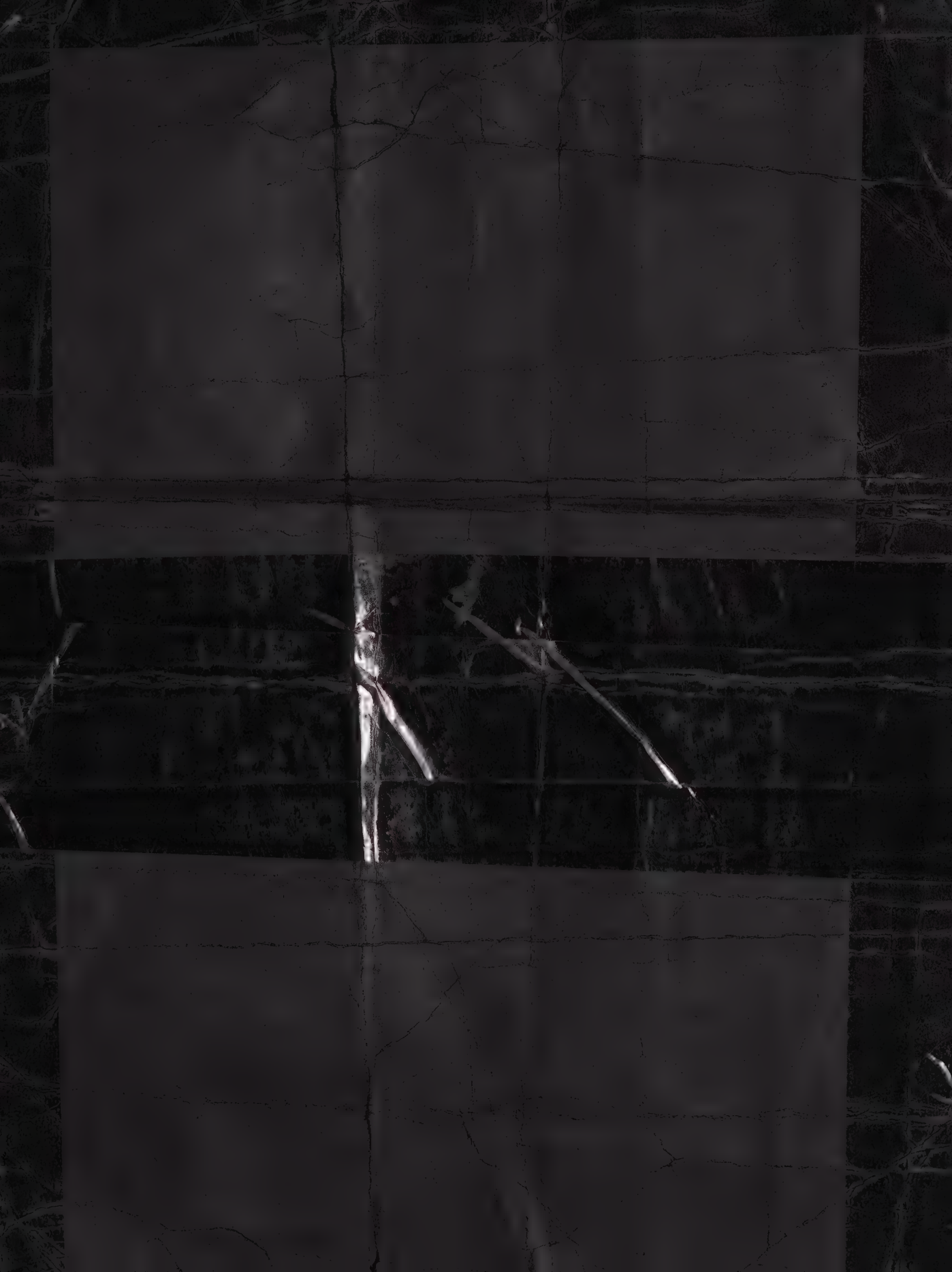
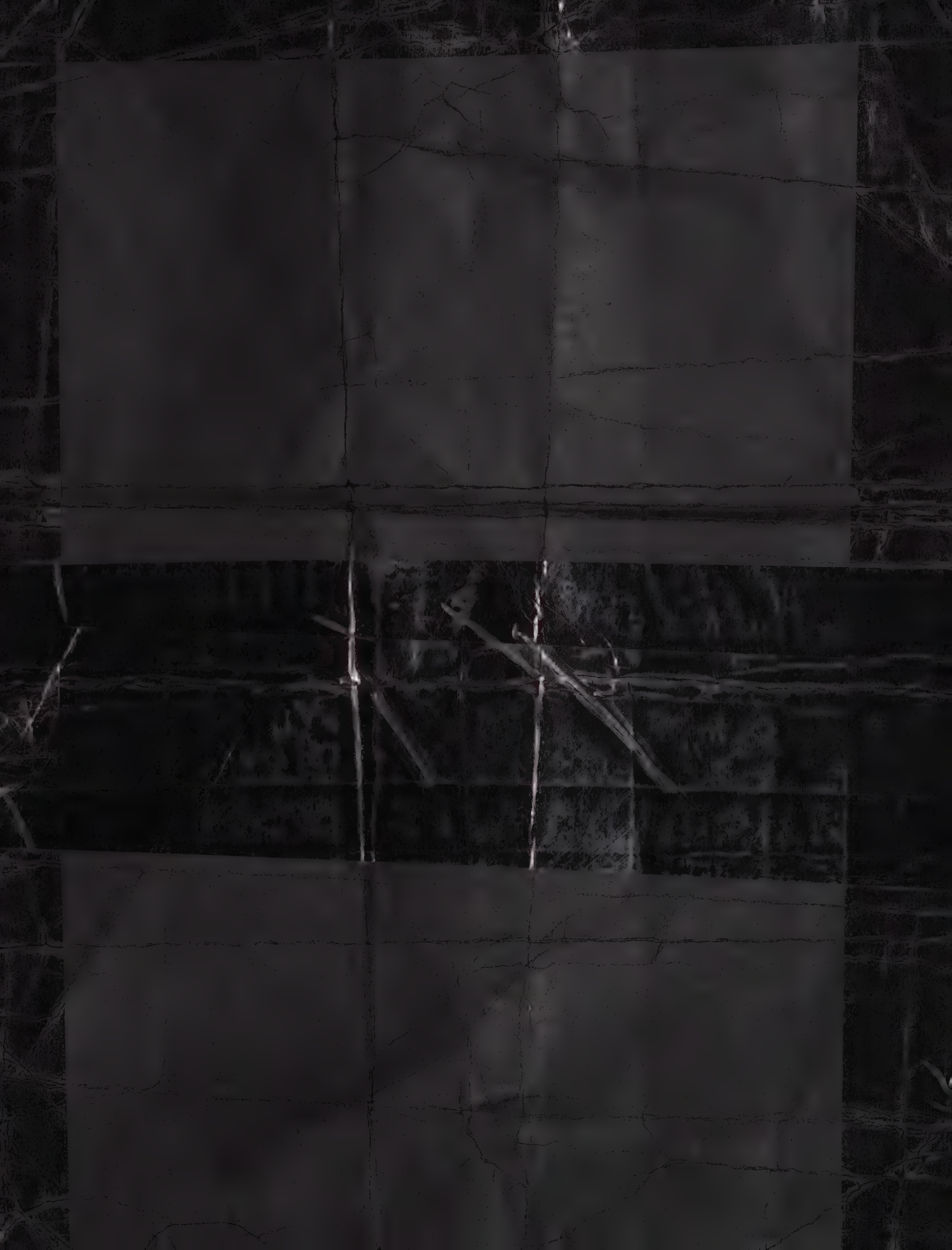


FIGURE 8.13





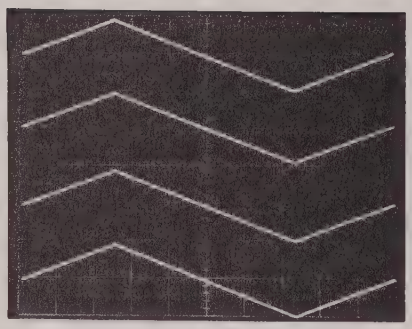


FIGURE 8.2

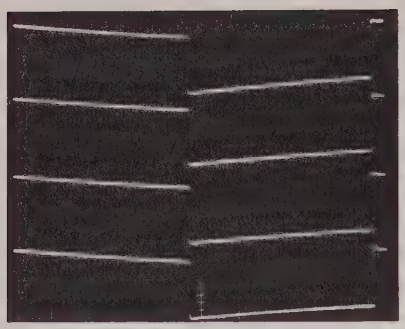


FIGURE 8.3

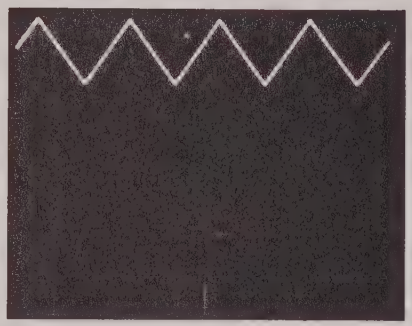


FIGURE 8.6

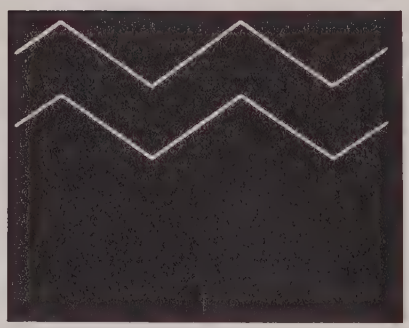


FIGURE 8.7

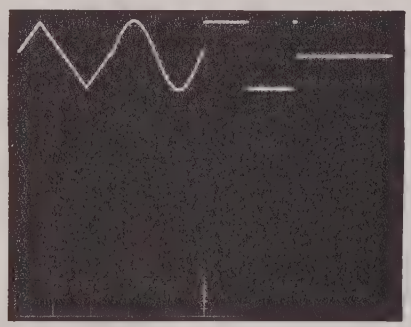


FIGURE 8.10

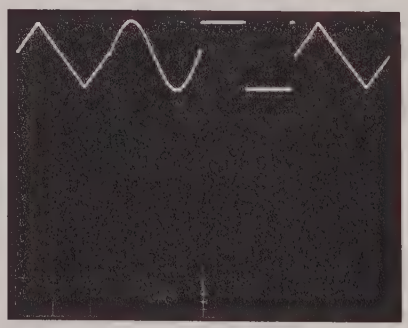


FIGURE 8.11

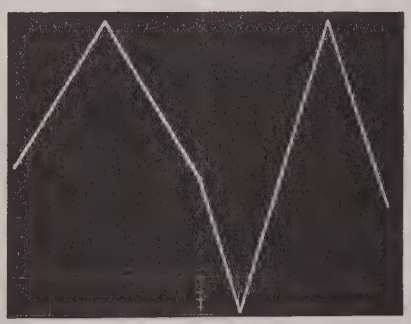


FIGURE 8.14

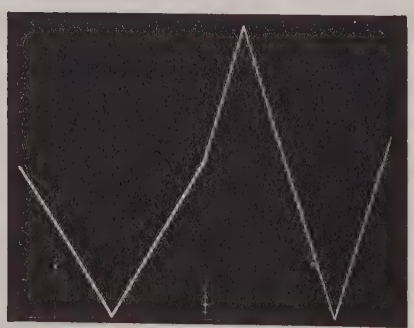
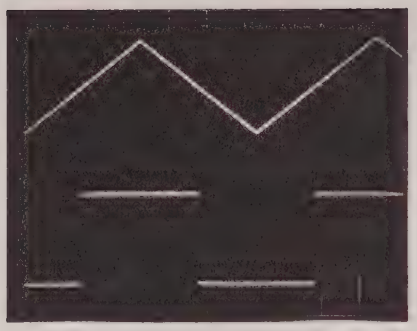


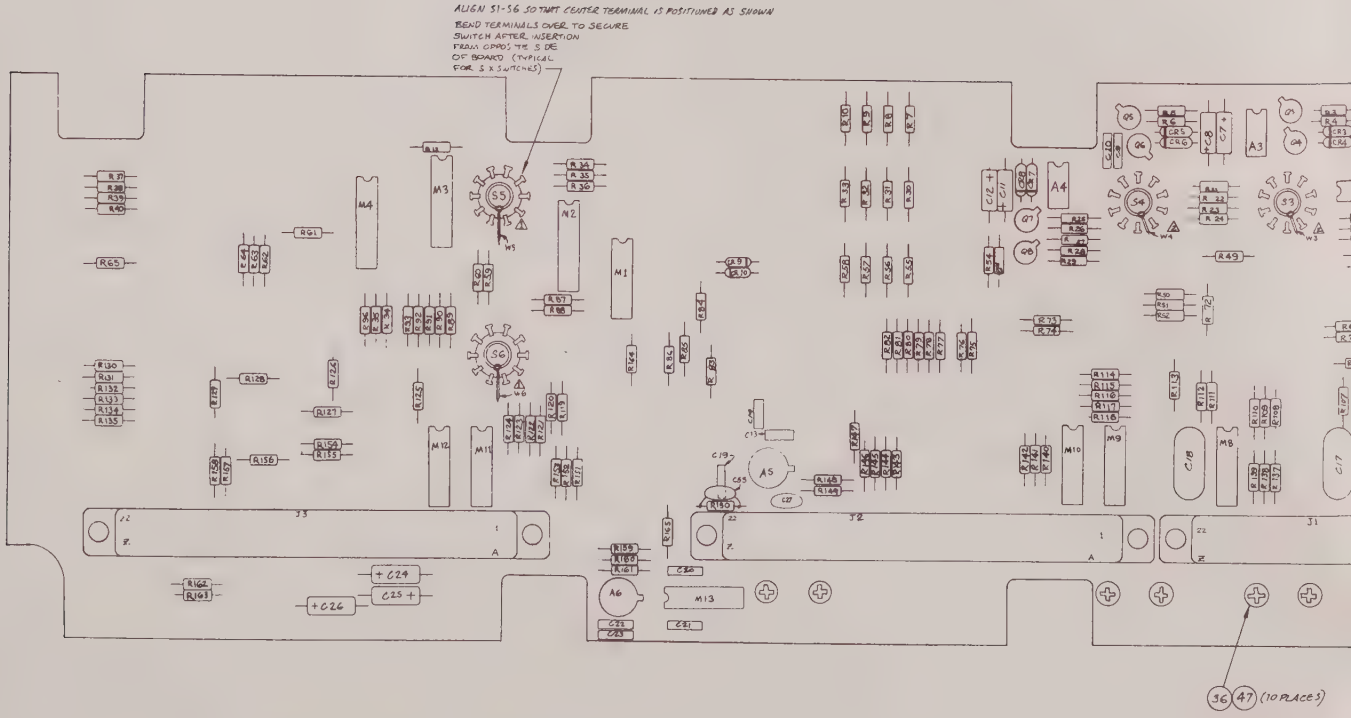
FIGURE 8.15

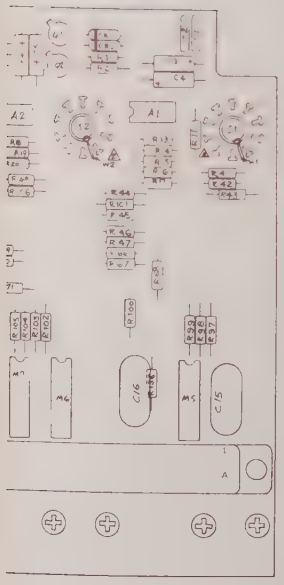
SECTION IX

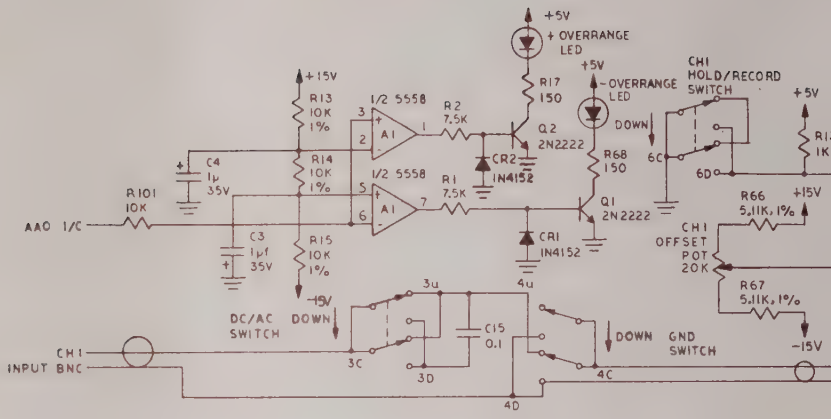
Schematics, Mechanical Drawings and Maintenance Diagnostic Illustrations

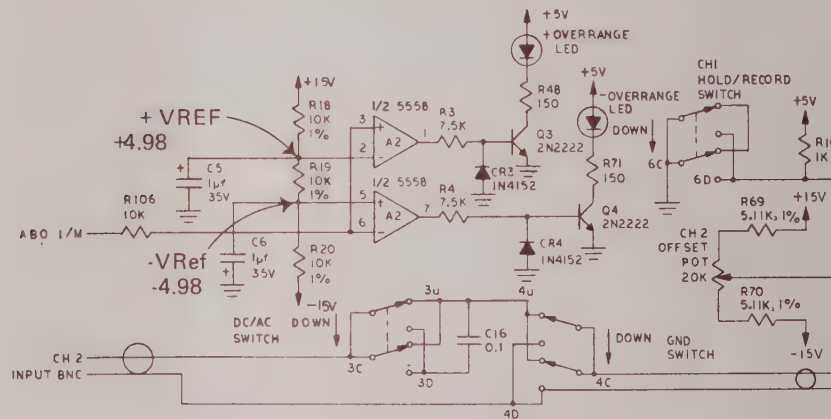


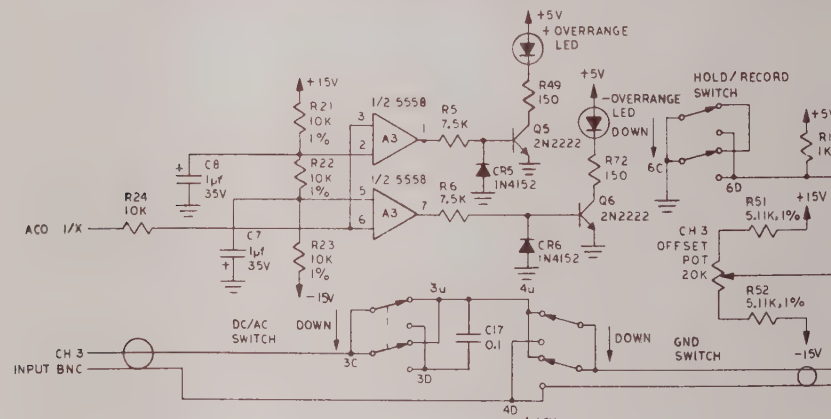
1. Scope: Vert. CH 1 10 v/div, CH 2 2 v/div, Horz. 2 msec/div. Trigger: Ext: Function Generator Sync.
   1015: Trig Level Mid-Range Function Generator Tri output 2 OV PP connected to Ext in BNC Trigger Source Ext.

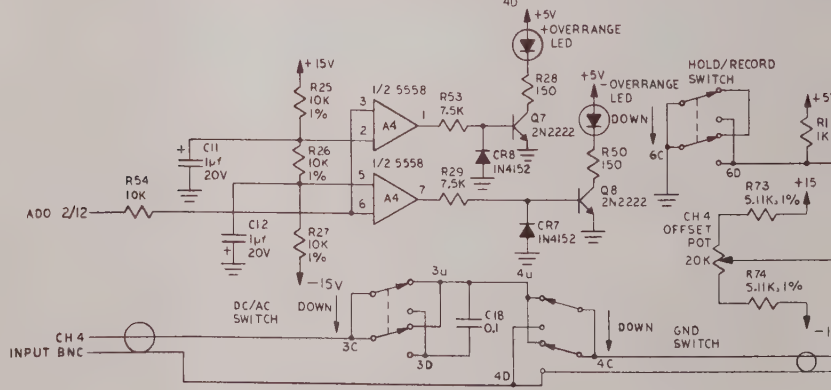


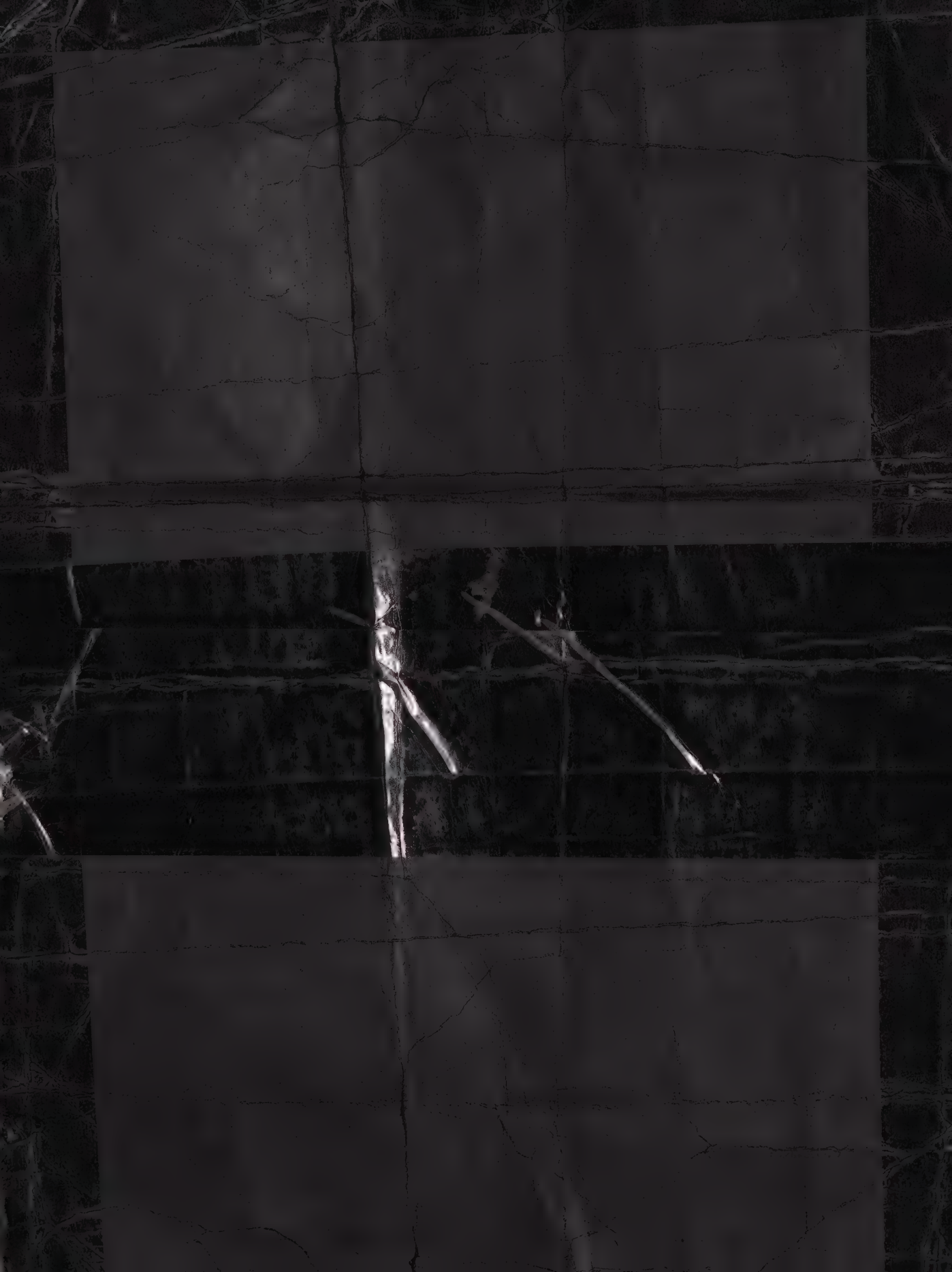


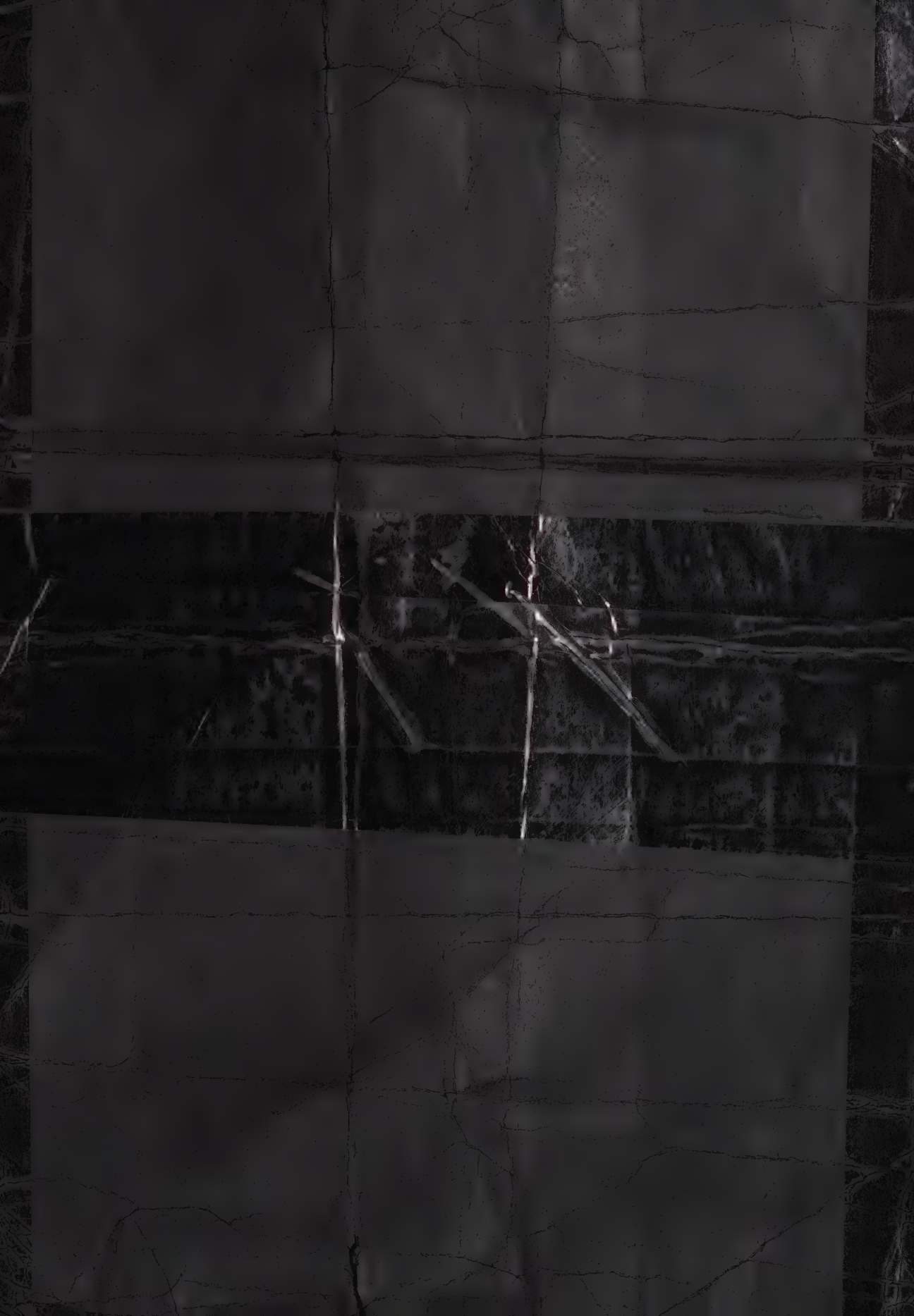

+5V
+ OVERRANGE LED
-OVERRANGE LED
CH1 HOLD/RECORD SWITCH
DOWN
R17 150
R68 150
Q2 2N2222
Q1 2N2222
CR2 IN4152
CR1 IN4152
R1 7.5K
R2 7.5K
1/2 5558
A1
+15V
R13 10K 1%
R14 10K 1%
R15 10K 1%
C4 1µ 35V
C3 1µf 35V
R101 10K
AAO I/C
-15V
DC/AC SWITCH
CH1 INPUT BNC
C15 0.1
GND SWITCH
R66 5.11K, 1%
R67 5.11K, 1%
CH1 OFFSET POT 20K
3u
4u
3C
3D
4C
4D
6C
6D

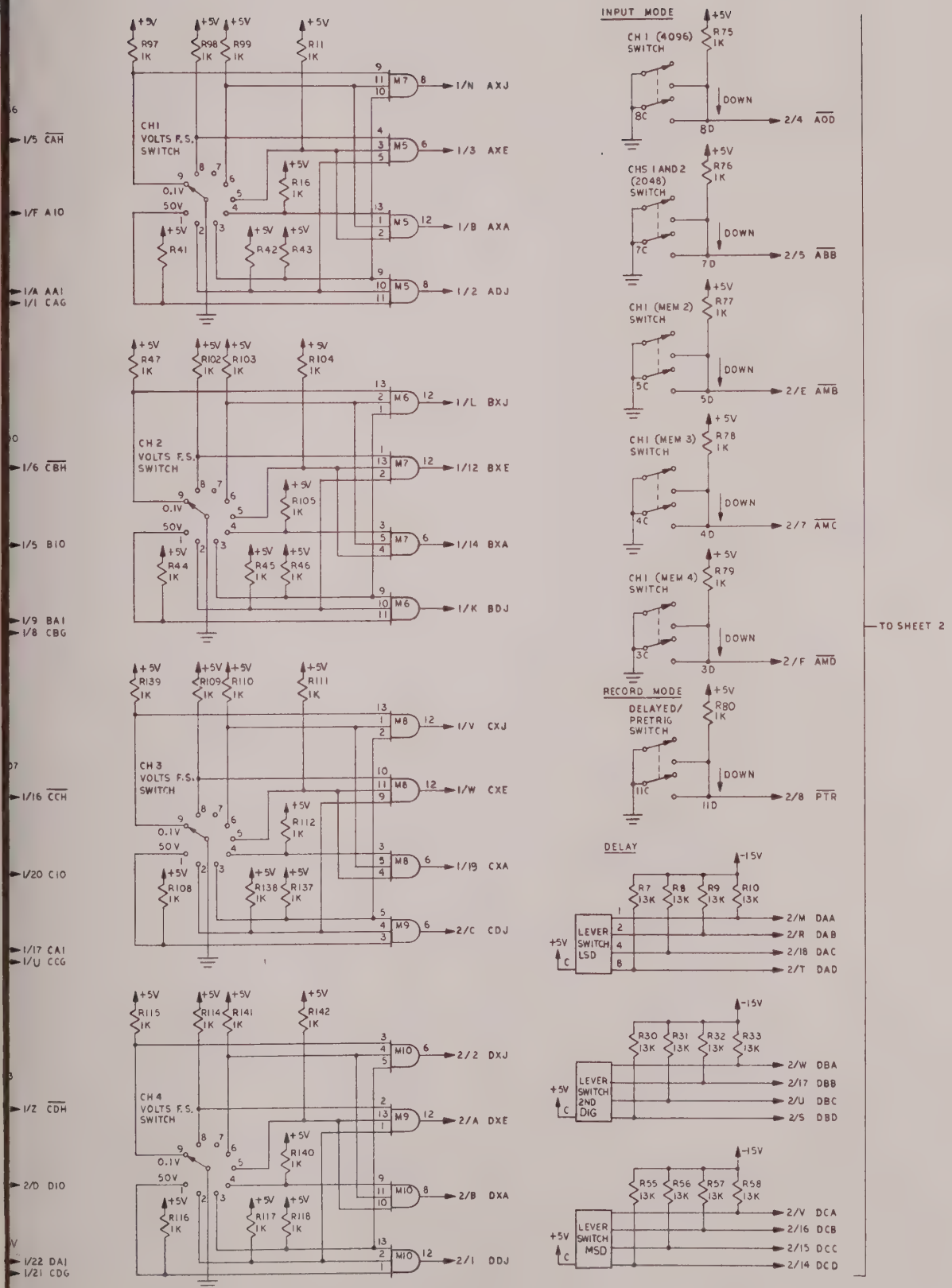

+5V
+ OVERRANGE LED
-OVERRANGE LED
CH1 HOLD/RECORD SWITCH
DOWN
R48 150
R71 150
Q3 2N2222
Q4 2N2222
CR3 IN4152
CR4 IN4152
R3 7.5K
R4 7.5K
1/2 5558
A2
+15V
R18 10K 1%
R19 10K 1%
R20 10K 1%
+ VREF
+4.98
-VRef
-4.98
C5 1µf 35V
C6 1µf 35V
R106 10K
ABO I/M
-15V
DC/AC SWITCH
CH 2 INPUT BNC
C16 0.1
GND SWITCH
R69 5.11K, 1%
R70 5.11K, 1%
CH 2 OFFSET POT 20K
3u
4u
3C
3D
4C
4D
6C
6D

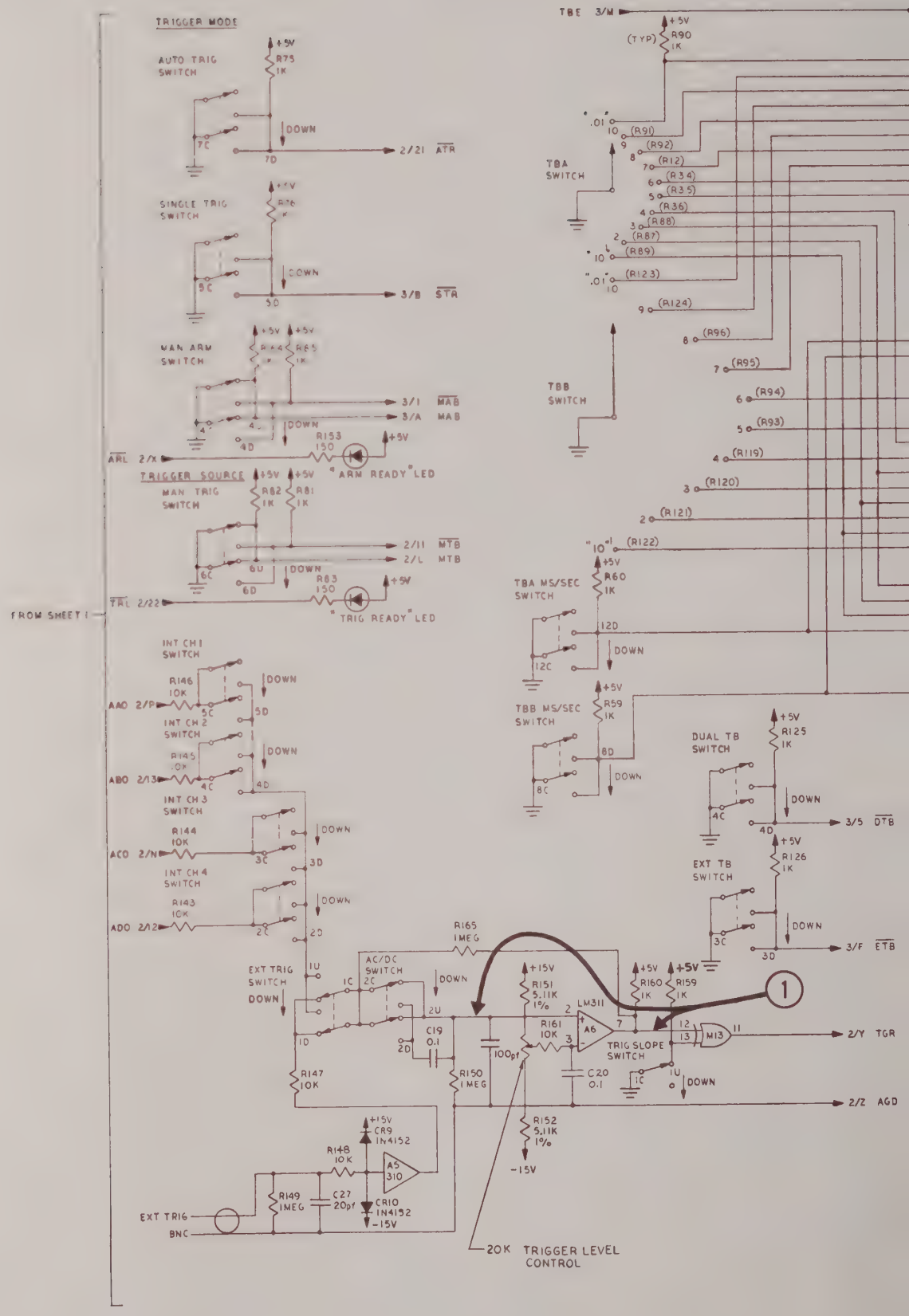

+5V
+ OVERRANGE LED
-OVERRANGE LED
HOLD/RECORD SWITCH
DOWN
R49 150
R72 150
Q5 2N2222
Q6 2N2222
CR5 IN4152
CR6 IN4152
R5 7.5K
R6 7.5K
1/2 5558
A3
+15V
R21 10K 1%
R22 10K 1%
R23 10K 1%
C8 1µf 35V
C7 1µf 35V
R24 10K
ACO I/X
-15V
DC/AC SWITCH
CH 3 INPUT BNC
C17 0.1
GND SWITCH
R51 5.11K, 1%
R52 5.11K, 1%
CH 3 OFFSET POT 20K
3u
4u
3C
3D
4C
4D
6C
6D

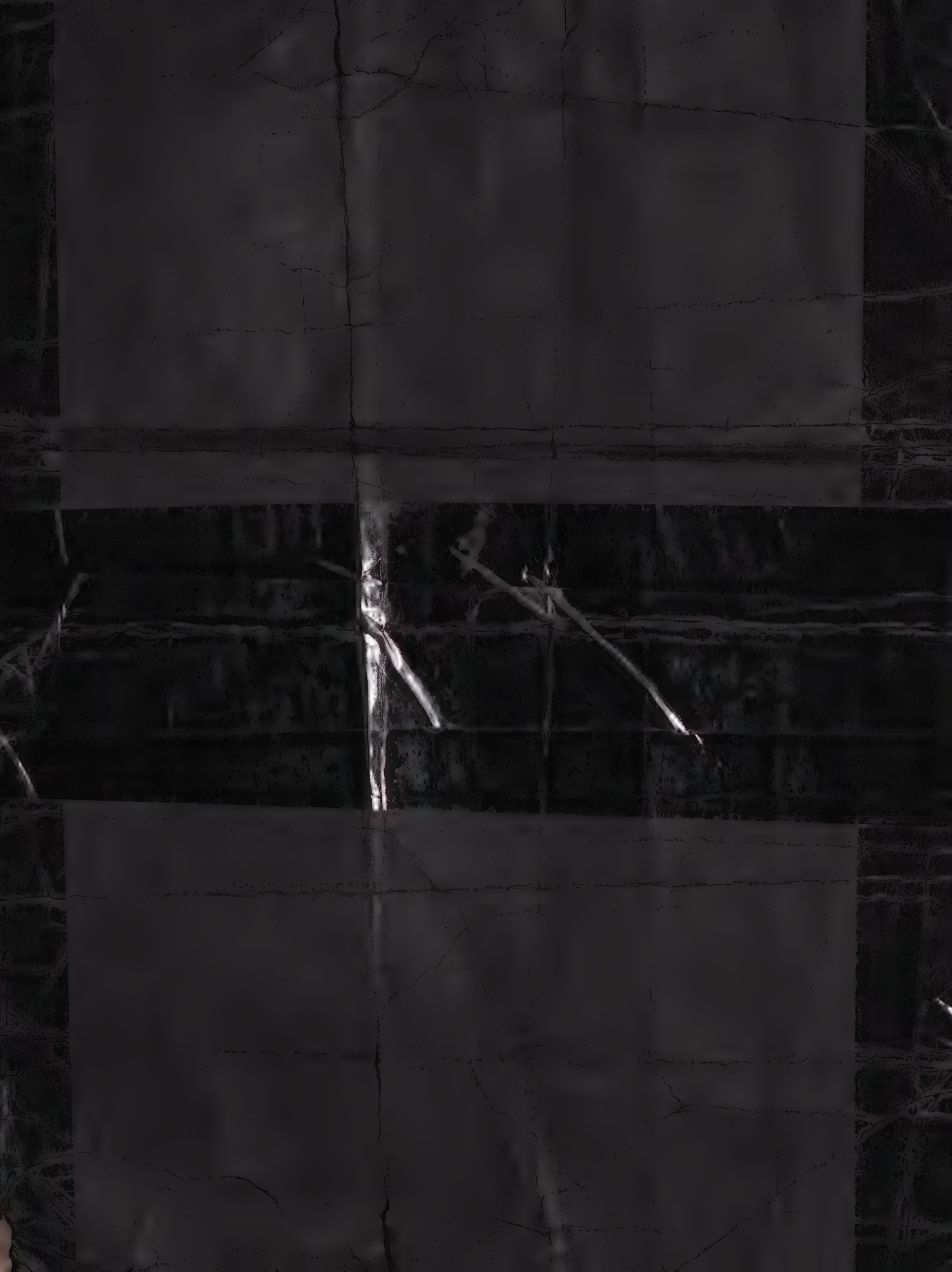

+5V
+OVERRANGE LED
-OVERRANGE LED
HOLD/RECORD SWITCH
DOWN
R28 150
R50 150
Q7 2N2222
Q8 2N2222
CR8 IN4152
CR7 IN4152
R53 7.5K
R29 7.5K
1/2 5558
A4
+15V
R25 10K 1%
R26 10K 1%
R27 10K 1%
C11 1µf 20V
C12 1µf 20V
R54 10K
ADO 2/12
-15V
DC/AC SWITCH
CH 4 INPUT BNC
C18 0.1
GND SWITCH
R73 5.11K, 1%
R74 5.11K, 1%
CH 4 OFFSET POT 20K
3u
4u
3C
3D
4C
4D
6C
6D

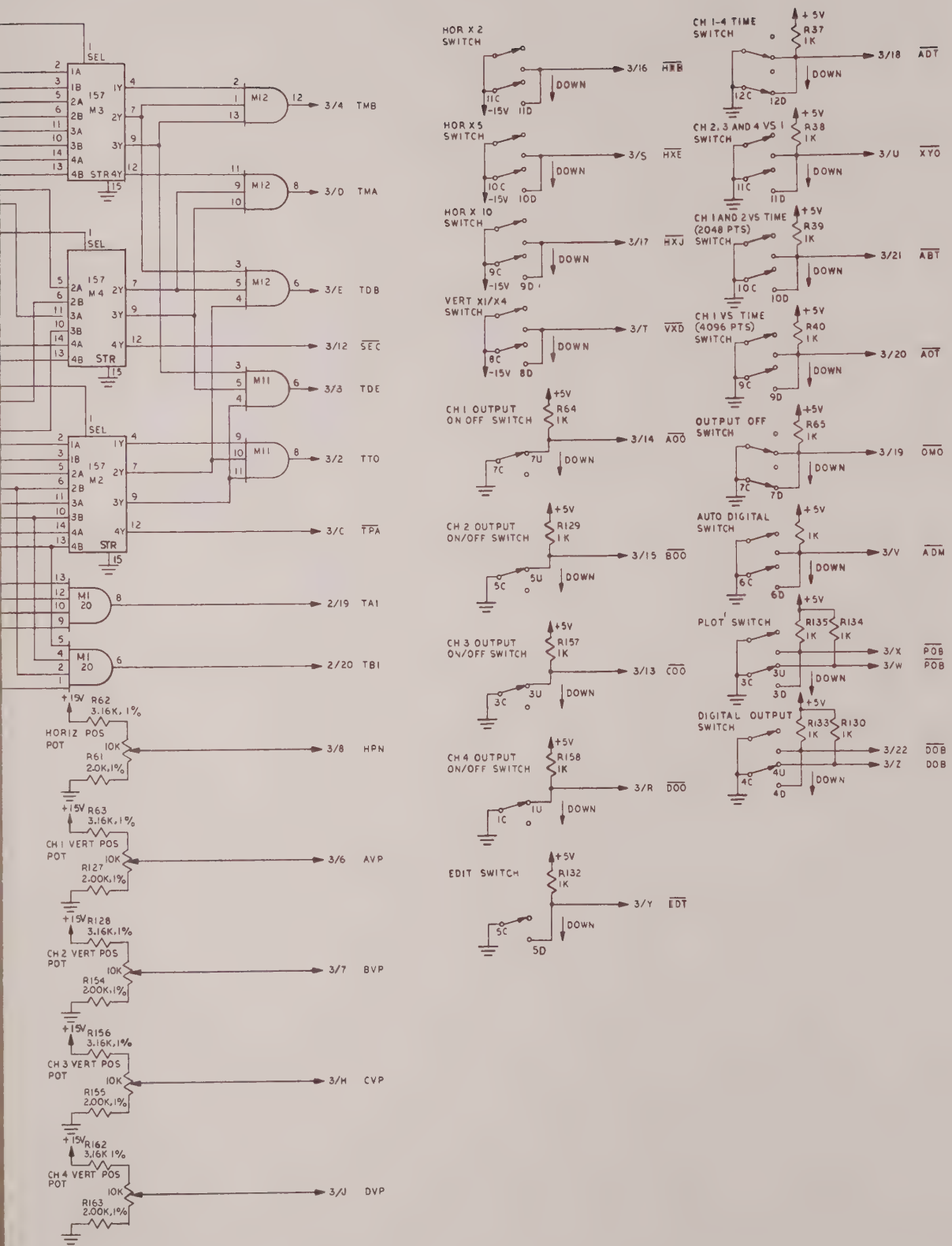


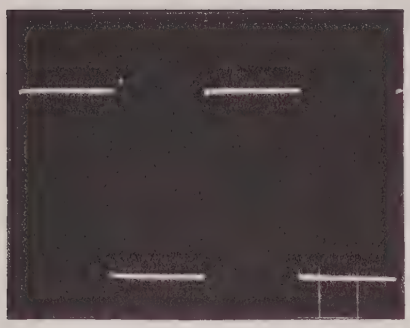



CH1 VOLTS F.S. SWITCH
CH2 VOLTS F.S. SWITCH
CH3 VOLTS F.S. SWITCH
CH4 VOLTS F.S. SWITCH
0.1V
50V
1/N AXJ
1/3 AXE
1/B AXA
1/2 ADJ
1/L BXJ
1/12 BXE
1/14 BXA
1/K BDJ
1/V CXJ
1/W CXE
1/19 CXA
2/C CDJ
2/2 DXJ
2/A DXE
2/B DXA
2/1 DDJ
INPUT MODE
CH 1 (4096) SWITCH
CHS 1 AND 2 (2048) SWITCH
CH1 (MEM 2) SWITCH
CH1 (MEM 3) SWITCH
CH1 (MEM 4) SWITCH
DOWN
2/4 AOD
2/5 ABB
2/E AMB
2/7 AMC
2/F AMD
RECORD MODE
DELAYED/ PRETRIG SWITCH
2/8 PTR
DELAY
LEVER SWITCH LSD
LEVER SWITCH 2ND DIG
LEVER SWITCH MSD
2/M DAA
2/R DAB
2/18 DAC
2/T DAD
2/W DBA
2/17 DBB
2/U DBC
2/S DBD
2/V DCA
2/16 DCB
2/15 DCC
2/14 DCD
TO SHEET 2

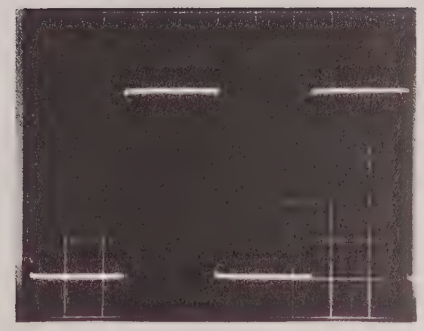

TRIGGER MODE
AUTO TRIG SWITCH
+5V
R75 1K
DOWN
7C
7D
2/21 ATR
SINGLE TRIG SWITCH
R76
DOWN
5C
5D
3/B STA
MAN ARM SWITCH
+5V
R84
R85 1K
3/1 MAB
3/A MAB
4C
4D
DOWN
R153 150
+5V
ARL 2/X
"ARM READY" LED
TRIGGER SOURCE
MAN TRIG SWITCH
R82 1K
R81 1K
2/11 MTB
2/L MTB
6C
6U
6D
DOWN
R83 150
+5V
TRL 2/22
"TRIG READY" LED
FROM SHEET 1
INT CH 1 SWITCH
R146 10K
DOWN
AAO 2/P
5C
5D
INT CH 2 SWITCH
R145 10K
DOWN
ABO 2/13
4C
4D
INT CH 3 SWITCH
R144 10K
DOWN
ACO 2/N
3C
3D
INT CH 4 SWITCH
R143 10K
DOWN
ADO 2/12
2C
2D
EXT TRIG SWITCH
DOWN
1C
1D
1U
AC/DC SWITCH
2C
2D
2U
DOWN
R165 1MEG
C19 0.1
100pf
R147 10K
R150 1MEG
+15V
R151 5.11K 1%
R161 10K
LM311
A6
TRIG SLOPE SWITCH
C20 0.1
1C
1U
DOWN
R152 5.11K 1%
-15V
+5V
R160 1K
R159 1K
M13
2/Y TGR
2/Z AGD
+15V
CR9 IN4152
R148 10K
A5 310
R149 1MEG
C27 20pf
CR10 IN4152
-15V
EXT TRIG BNC
20K TRIGGER LEVEL CONTROL
TBE 3/M
+5V
(TYP) R90 1K
.01
10
(R91)
9
(R92)
8
(R12)
7
(R34)
6
(R35)
5
(R36)
4
(R88)
3
(R87)
2
(R89)
.01
10
(R123)
9
(R124)
TBA SWITCH
8
(R96)
7
(R95)
6
(R94)
5
(R93)
4
(R119)
3
(R120)
2
(R121)
10
1
(R122)
TBB SWITCH
TBA MS/SEC SWITCH
+5V
R60 1K
12D
12C
DOWN
TBB MS/SEC SWITCH
+5V
R59 1K
8D
8C
DOWN
DUAL TB SWITCH
+5V
R125 1K
DOWN
4C
4D
3/5 DTB
EXT TB SWITCH
+5V
R126 1K
DOWN
3C
3D
3/F ETB



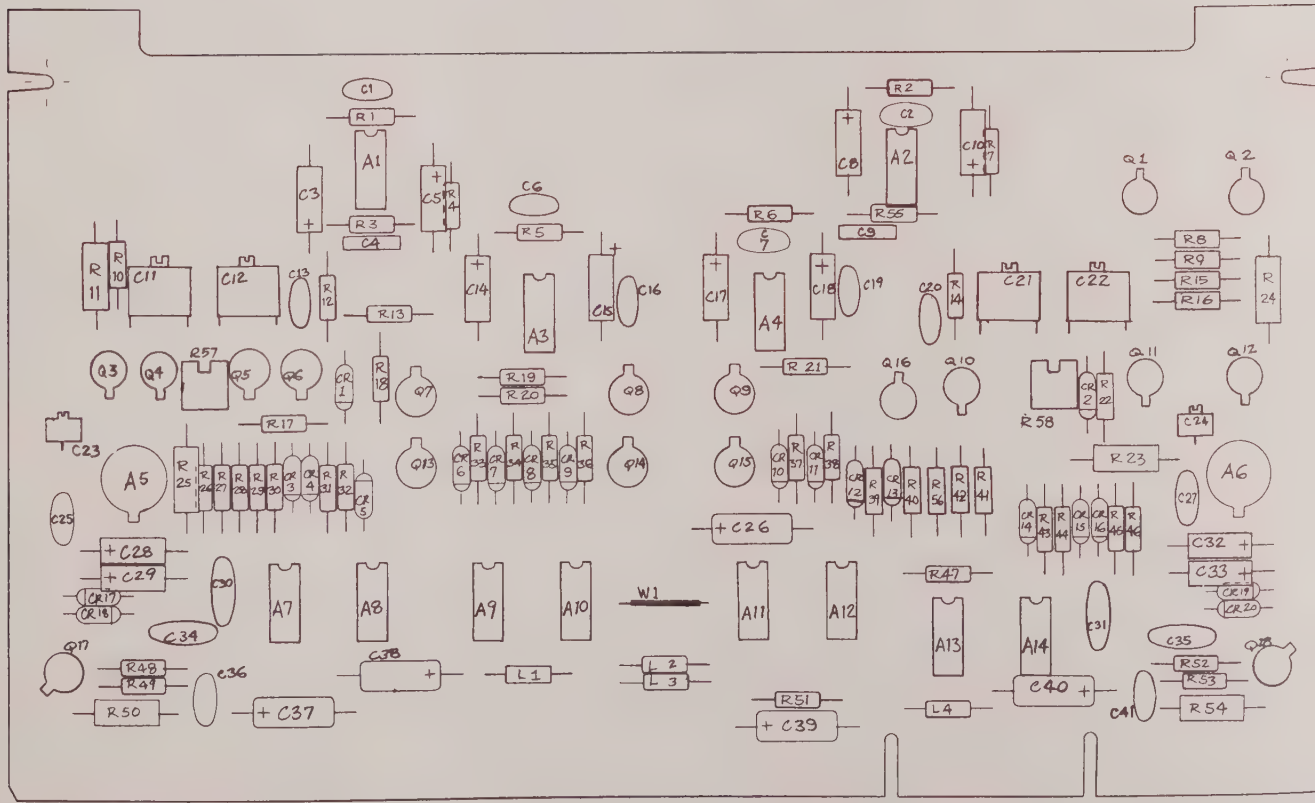

SEL
157 M3
157 M4
157 M2
STR
M12
M11
M1 20
3/4 TMB
3/D TMA
3/E TDB
3/12 SEC
3/3 TDE
3/2 TTO
3/C TPA
2/19 TA1
2/20 TB1
+15V R62 3.16K, 1%
HORIZ POS POT
10K
R61 2.0K, 1%
3/8 HPN
+15V R63 3.16K, 1%
CH 1 VERT POS POT
R127 2.00K, 1%
3/6 AVP
+15V R128 3.16K, 1%
CH 2 VERT POS POT
R154 2.00K, 1%
3/7 BVP
+15V R156 3.16K, 1%
CH 3 VERT POS POT
R155 2.00K, 1%
3/H CVP
+15V R162 3.16K 1%
CH 4 VERT POS POT
R163 2.00K, 1%
3/J DVP
HOR X 2 SWITCH
3/16 HXB
HOR X 5 SWITCH
3/S HXE
HOR X 10 SWITCH
3/17 HXJ
VERT X1/X4 SWITCH
3/T VXD
CH 1 OUTPUT ON OFF SWITCH
3/14 AOO
CH 2 OUTPUT ON/OFF SWITCH
3/15 BOO
CH 3 OUTPUT ON/OFF SWITCH
3/13 COO
CH 4 OUTPUT ON/OFF SWITCH
3/R DOO
EDIT SWITCH
3/Y EDT
+5V
DOWN
-15V
CH 1-4 TIME SWITCH
R37 1K
3/18 ADT
CH 2, 3 AND 4 VS 1 SWITCH
R38 1K
3/U XYO
CH 1 AND 2 VS TIME (2048 PTS) SWITCH
R39 1K
3/21 ABT
CH 1 VS TIME (4096 PTS) SWITCH
R40 1K
3/20 AOT
OUTPUT OFF SWITCH
R65 1K
3/19 OMO
AUTO DIGITAL SWITCH
3/V ADM
PLOT SWITCH
R135 1K
R134 1K
3/X POB
3/W POB
DIGITAL OUTPUT SWITCH
R133 1K
R130 1K
3/22 DOB
3/Z DOB

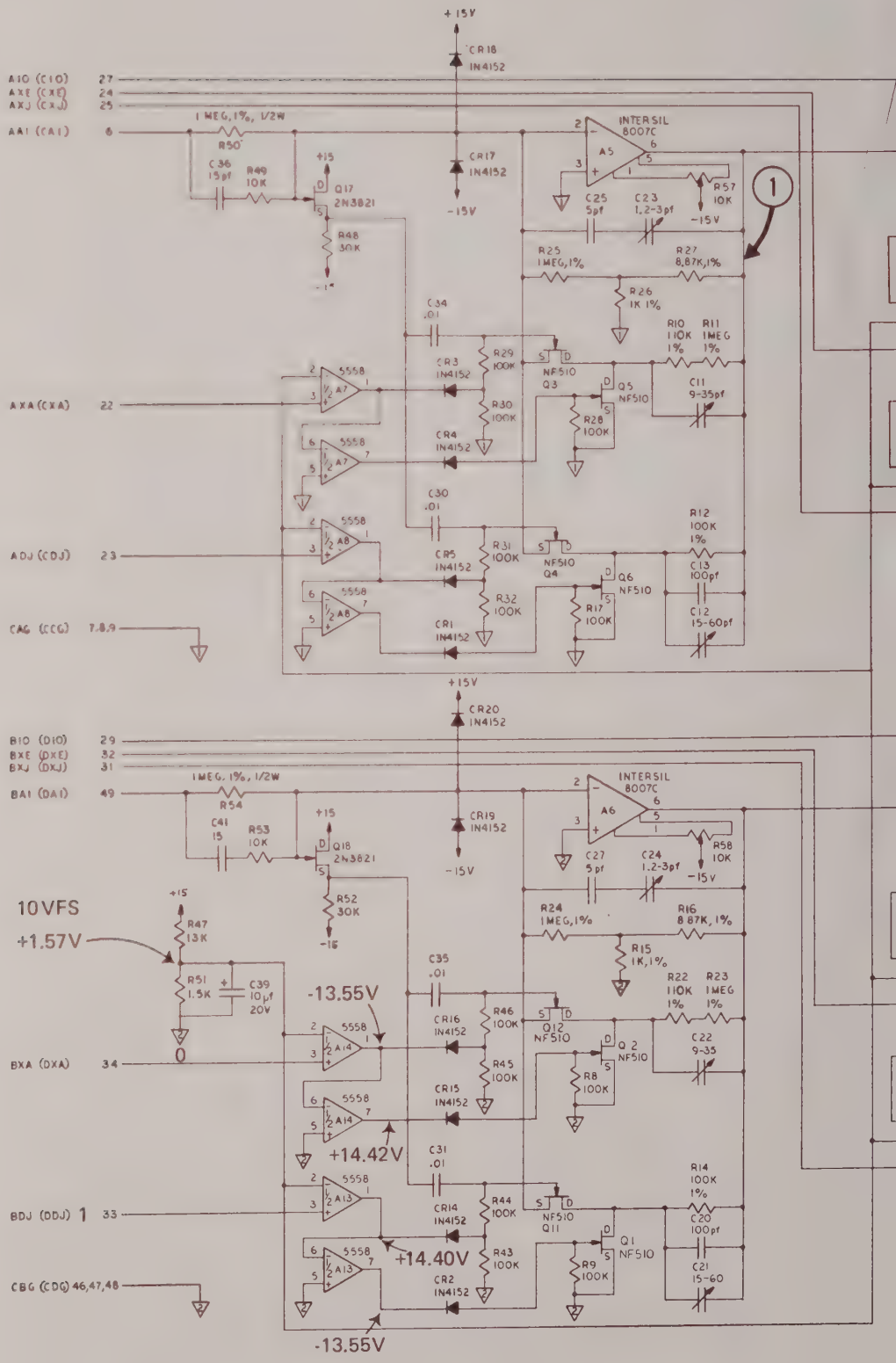


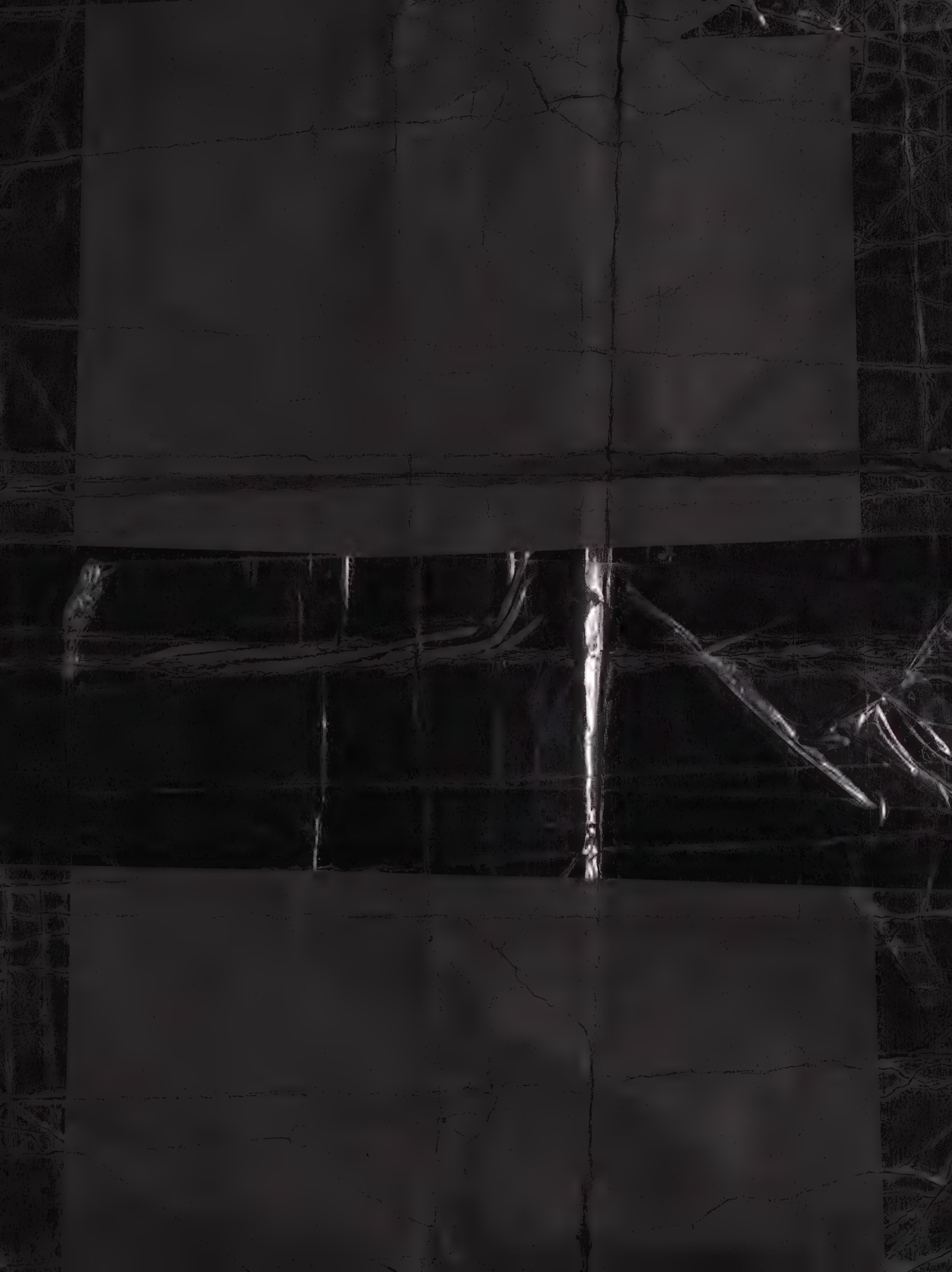
1. Scope: Vert .2 v/div, Horz. 2 msec/div.
   Trigger: Ext on function Gen. Sync.
   1015: CH 1 VFS 10, offset midrange, DC coupling – input 10 VPP sq. wave.

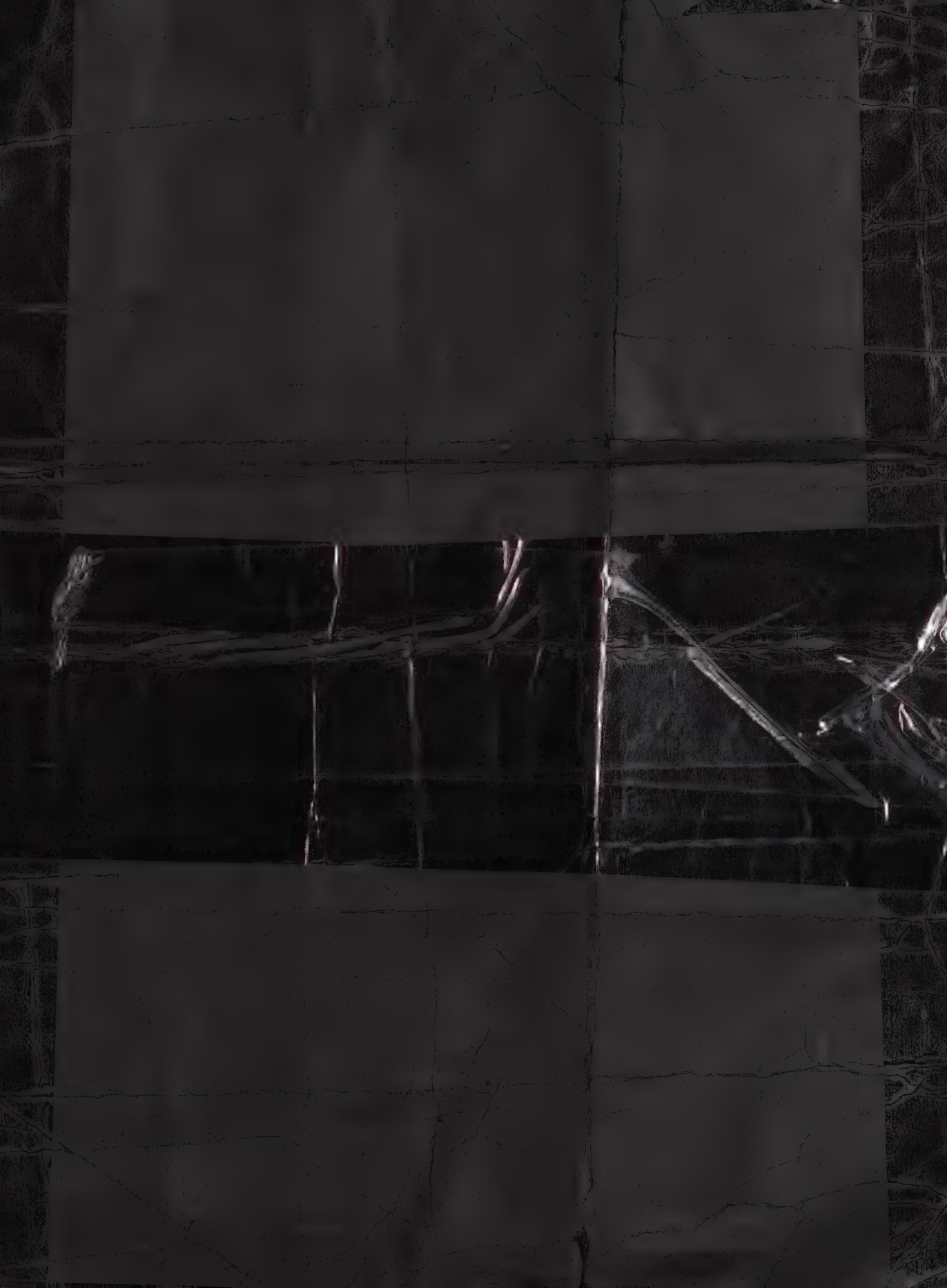


2. Scope: Vert. 2 v/div, Horz. 2 msec/div.
   Trigger: Ext on function Gen. Sync.
   1015: CH 1 VFS 10 offset midrange DC coupling – input 10 VPP sq. wave.



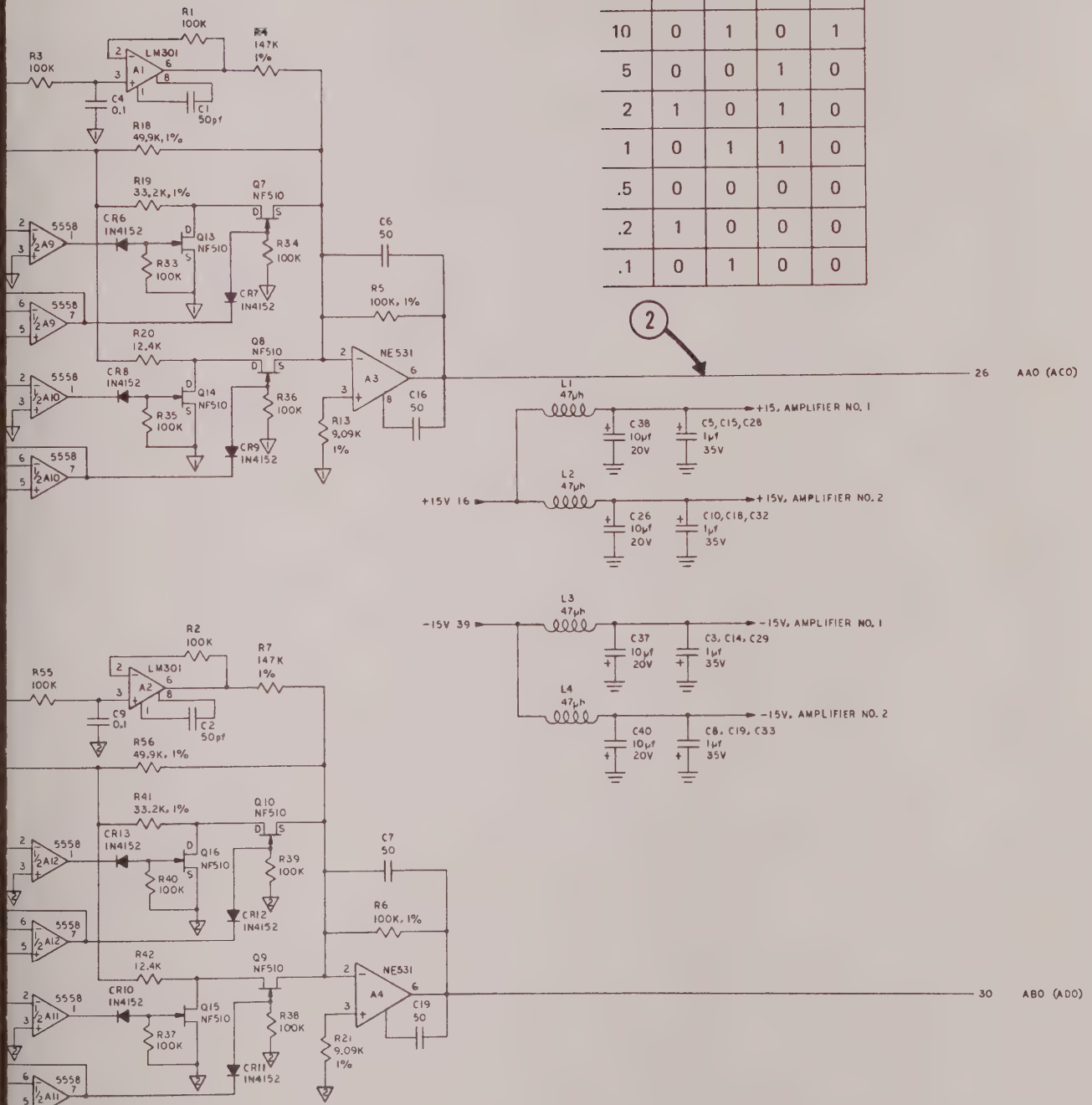

+15V
CR18 IN4152
AIO (CIO) 27
AXE (CXE) 24
AXJ (CXJ) 25
AAI (CAI) 6
1 MEG, 1%, 1/2W
R50
C36 15pf
R49 10K
Q17 2N3821
R48 30K
CR17 IN4152
-15V
INTERSIL 8007C
A5
C25 5pf
C23 1.2-3pf
R57 10K
R25 1MEG, 1%
R27 8.87K, 1%
R26 1K 1%
C34 .01
R10 110K 1%
R11 1MEG 1%
AXA (CXA) 22
5558 A7
CR3 IN4152
R29 100K
R30 100K
NF510 Q3
Q5 NF510
R28 100K
C11 9-35pf
CR4 IN4152
C30 .01
ADJ (CDJ) 23
5558 A8
CR5 IN4152
R31 100K
NF510 Q4
Q6 NF510
R12 100K 1%
C13 100pf
R32 100K
R17 100K
C12 15-60pf
CAG (CCG) 7,8,9
CR1 IN4152
+15V
CR20 IN4152
BIO (DIO) 29
BXE (DXE) 32
BXJ (DXJ) 31
BAI (DAI) 49
1MEG, 1%, 1/2W
R54
C41 15
R53 10K
Q18 2N3821
R52 30K
CR19 IN4152
-15V
INTERSIL 8007C
A6
C27 5pf
C24 1.2-3pf
R58 10K
10VFS
+1.57V
R47 13K
R51 1.5K
C39 10pf 20V
R24 1MEG, 1%
R16 8.87K, 1%
R15 1K, 1%
C35 .01
-13.55V
R22 110K 1%
R23 1MEG 1%
CR16 IN4152
R46 100K
Q12 NF510
Q2 NF510
C22 9-35
BXA (DXA) 34
R45 100K
R8 100K
CR15 IN4152
+14.42V
C31 .01
R14 100K 1%
BDJ (DDJ) 1 33
CR14 IN4152
R44 100K
NF510 Q11
Q1 NF510
C20 100pf
+14.40V
R43 100K
R9 100K
C21 15-60
CBG (CDG) 46,47,48
CR2 IN4152
-13.55V

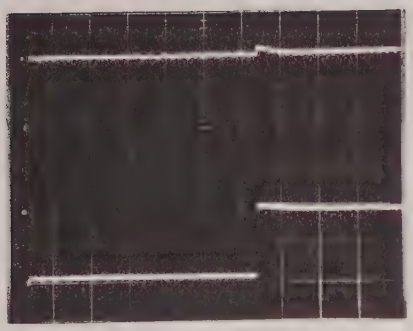




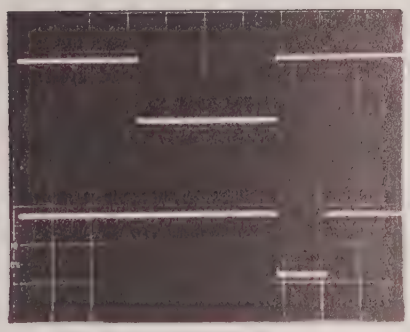
INPUT RANGE TRUTH TABLE

VFS	XE	XJ	XA	DJ
50	0	0	0	1
20	1	0	0	1
10	0	1	0	1
5	0	0	1	0
2	1	0	1	0
1	0	1	1	0
.5	0	0	0	0
.2	1	0	0	0
.1	0	1	0	0

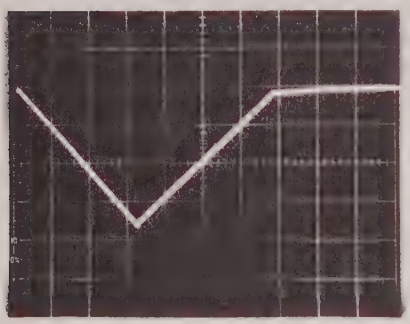




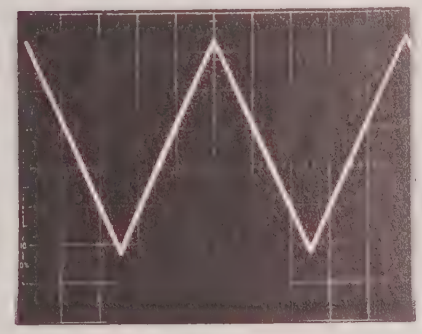
1. Scope: Vert. CH 1 & 2 2 v/div, Horz. .5μsec/div.
   Trigger: Int on CH 1 (c̄ōc̄).
   1015: Pre trig record, sample interval .01msec, unit armed, offset full CCW.



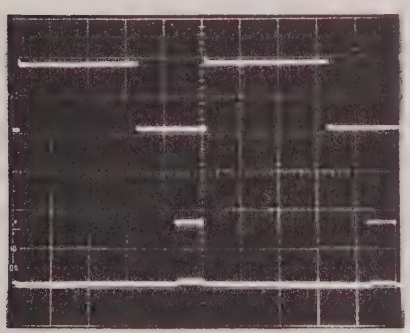
2. Scope: Vert. CH 1 & 2 2 v/div, Horz. 1μsec/div.
   Trigger: Ext on c̄ōc̄ – slope.
   1015: Pre trig record, sample interval .01 msec, unit armed, offset full CCW.



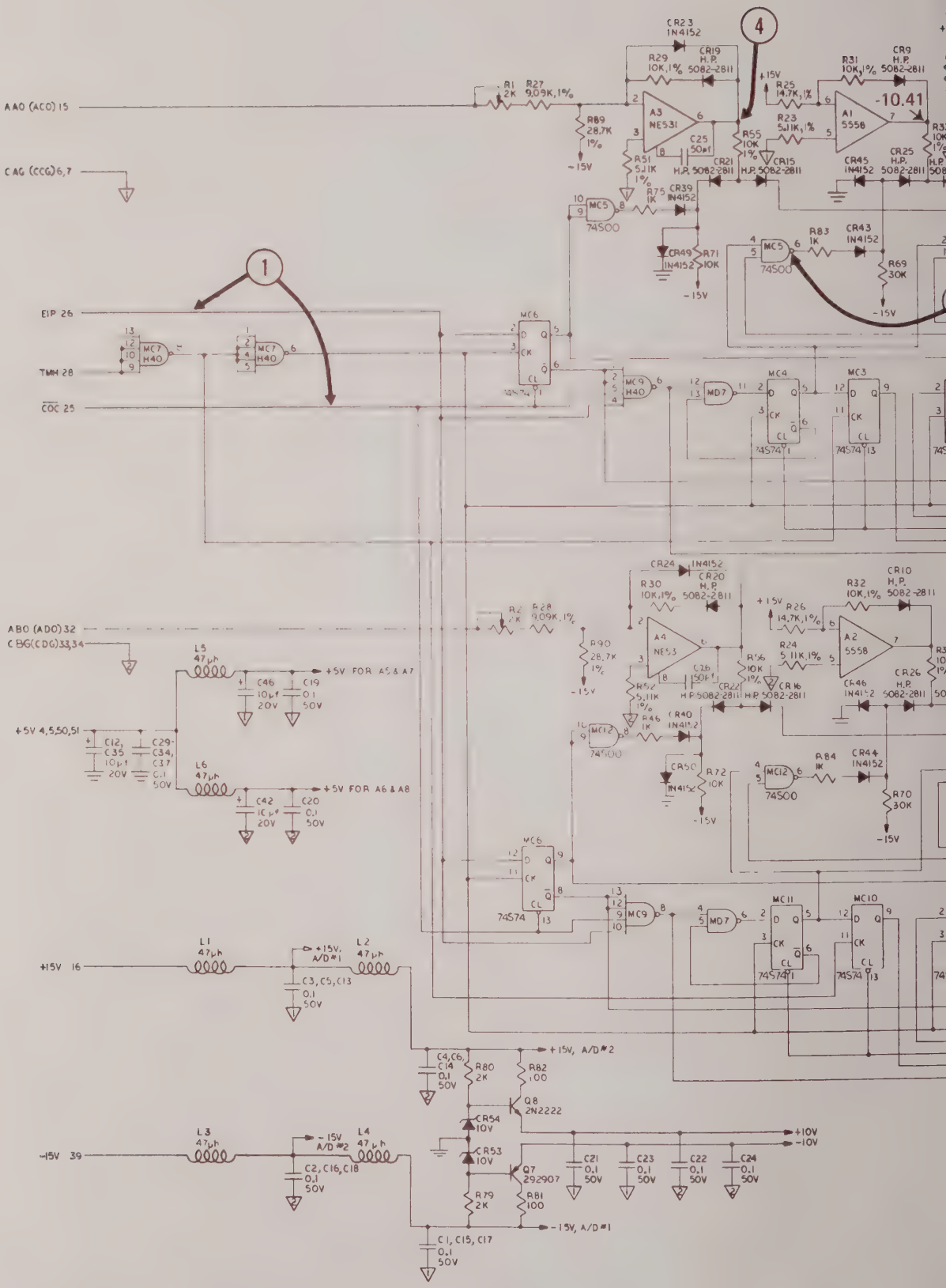
3. Scope: Vert. 1 v/div, Horz. 1 μsec/div.
   Trigger: Ext on c̄ōc̄ – slope.
   1015: Pre trig record, sample interval .01msec, unit armed, offset full CCW.

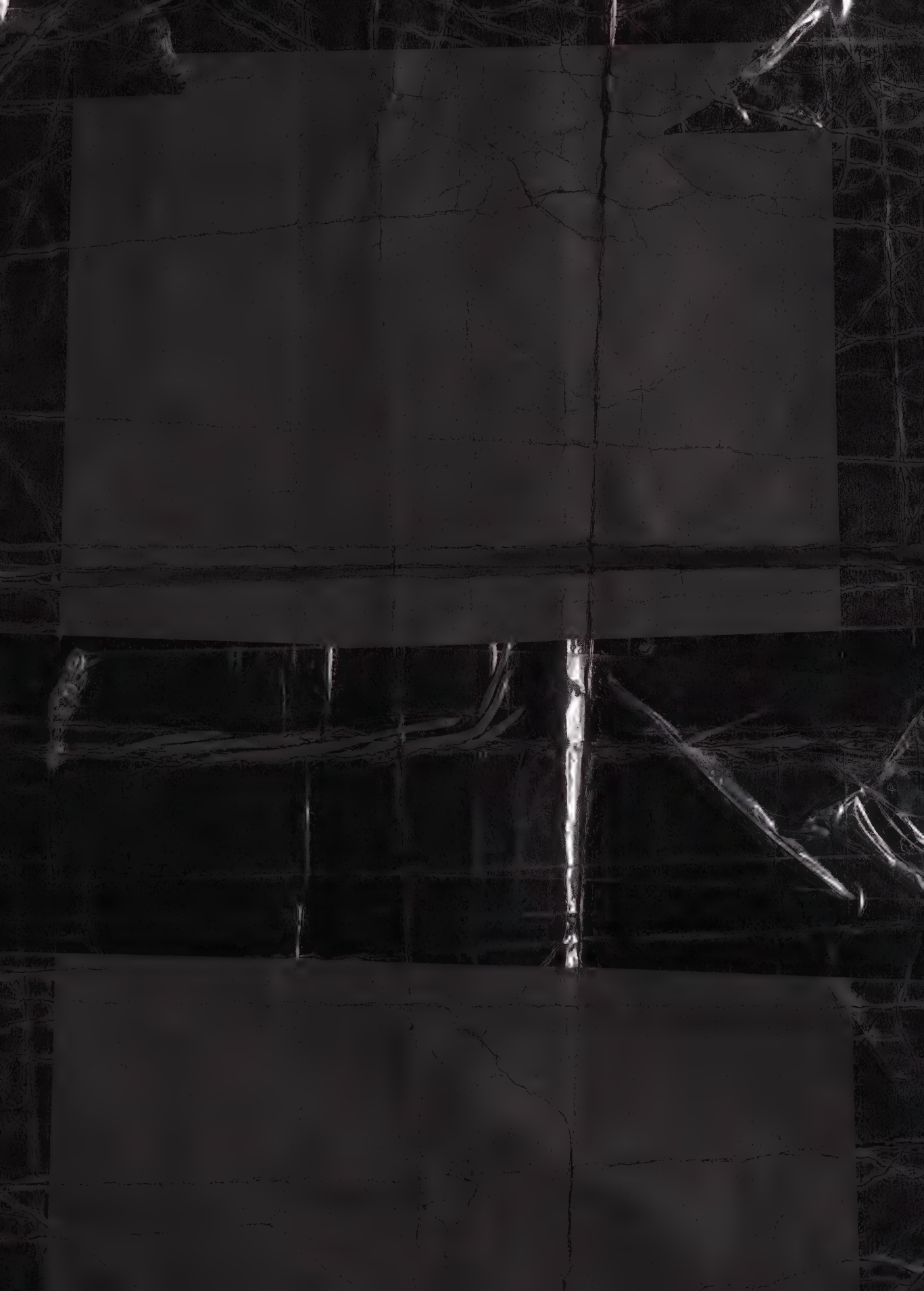


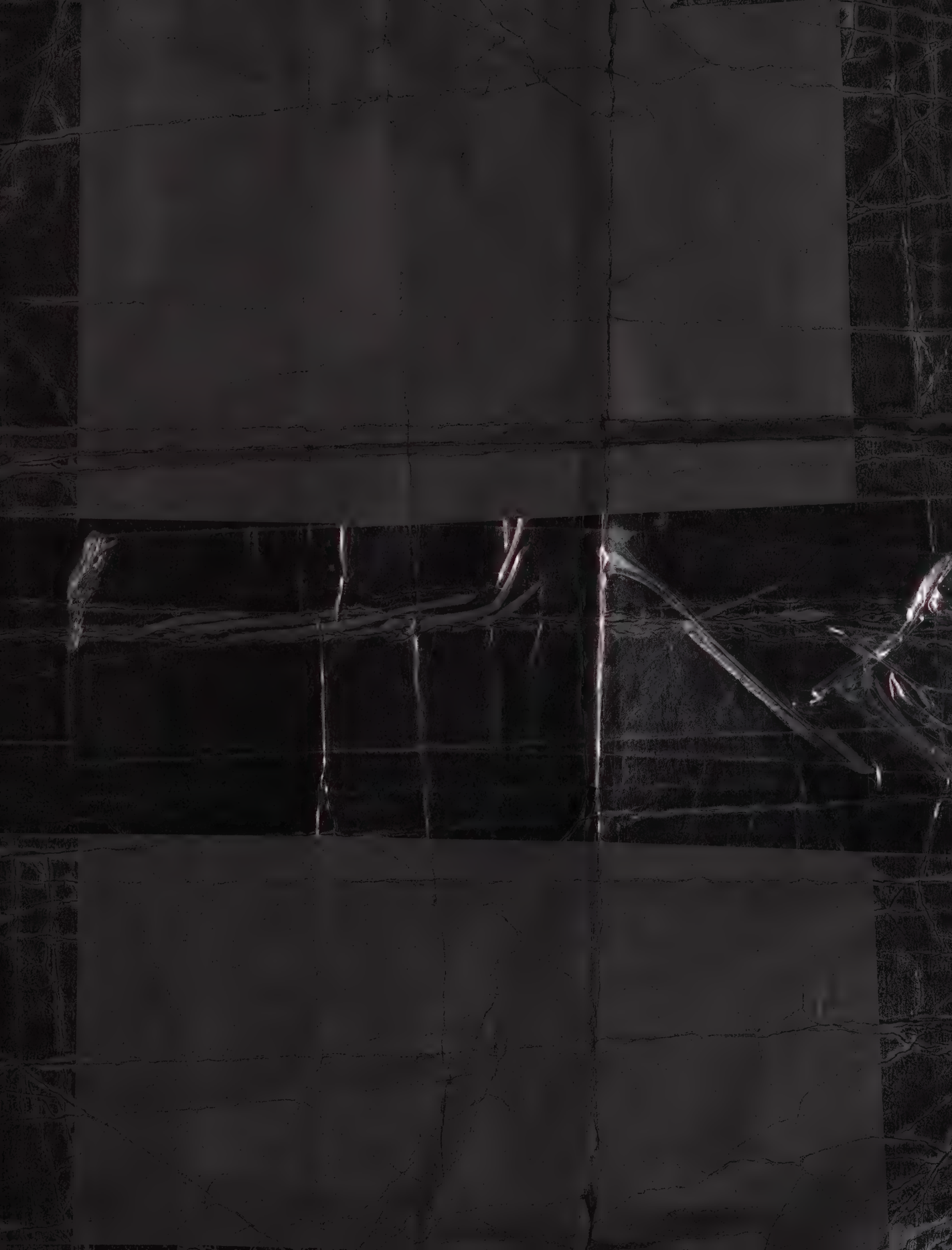
4. Scope: Vert. 2 v/div, Horz. 2 msec/div.
   Trigger: Ext on functions Gen sync.
   1015: 10 vfs offset midrange DC coupling.

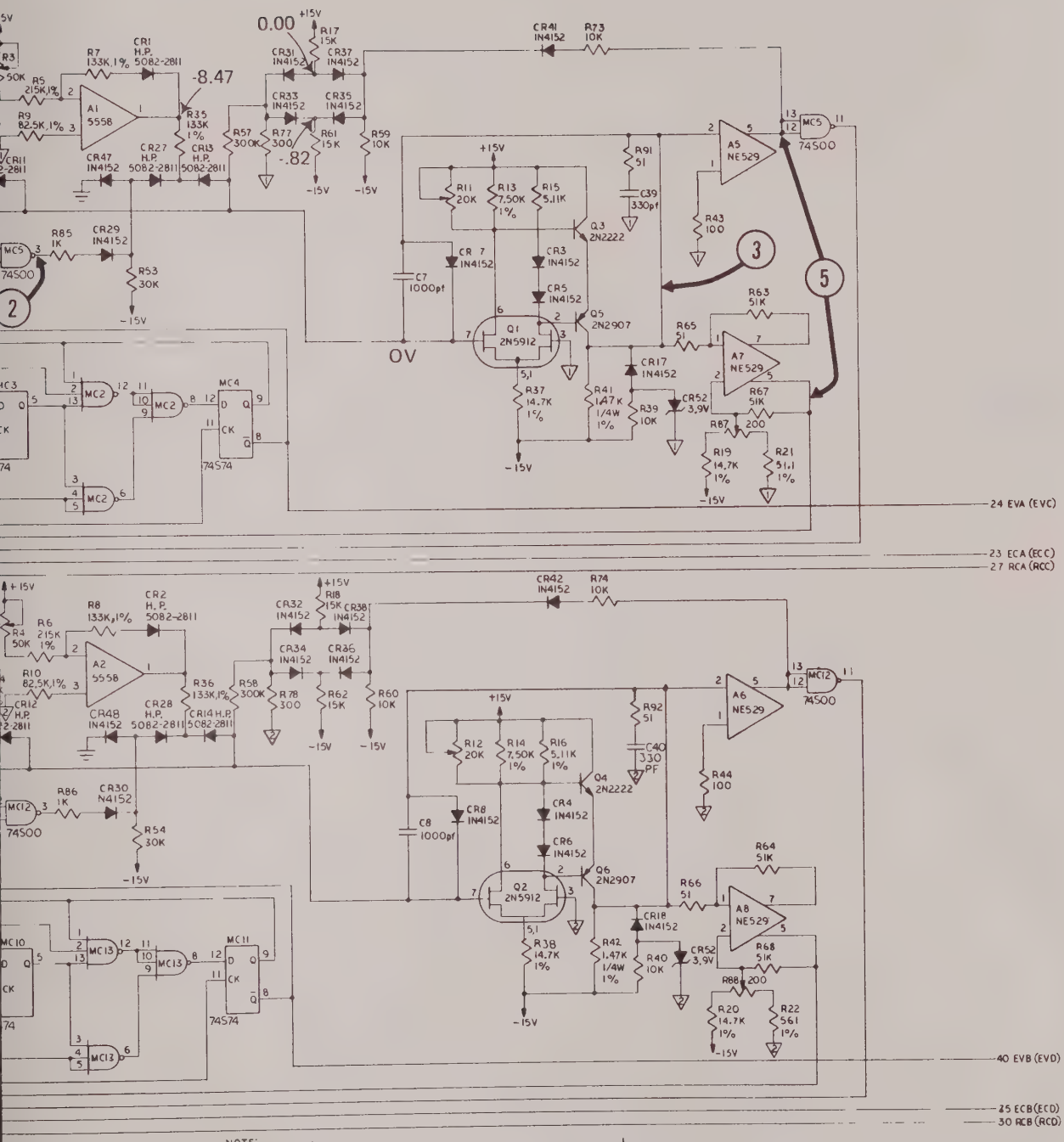


5. Scope: Vert. CH 1 & 2 2 v/div, Horz. 2μsec/div.
   Trigger: Ext on c̄ōc̄ – slope.
   1015: Pre trig record, sample interval .01msec, unit armed, offset full CCW.


AAO (ACO) 15
CAG (CCG) 6,7
EIP 26
TWH 28
COC 25
ABO (ADO) 32
CBG (CDG) 33,34
+5V 4,5,50,51
+15V 16
-15V 39
+5V FOR A5 & A7
+5V FOR A6 & A8
+15V, A/D#1
+15V, A/D#2
-15V, A/D#2
-15V, A/D#1
+10V
-10V
-10.41
74S00
74S74
74S74-1
1
4

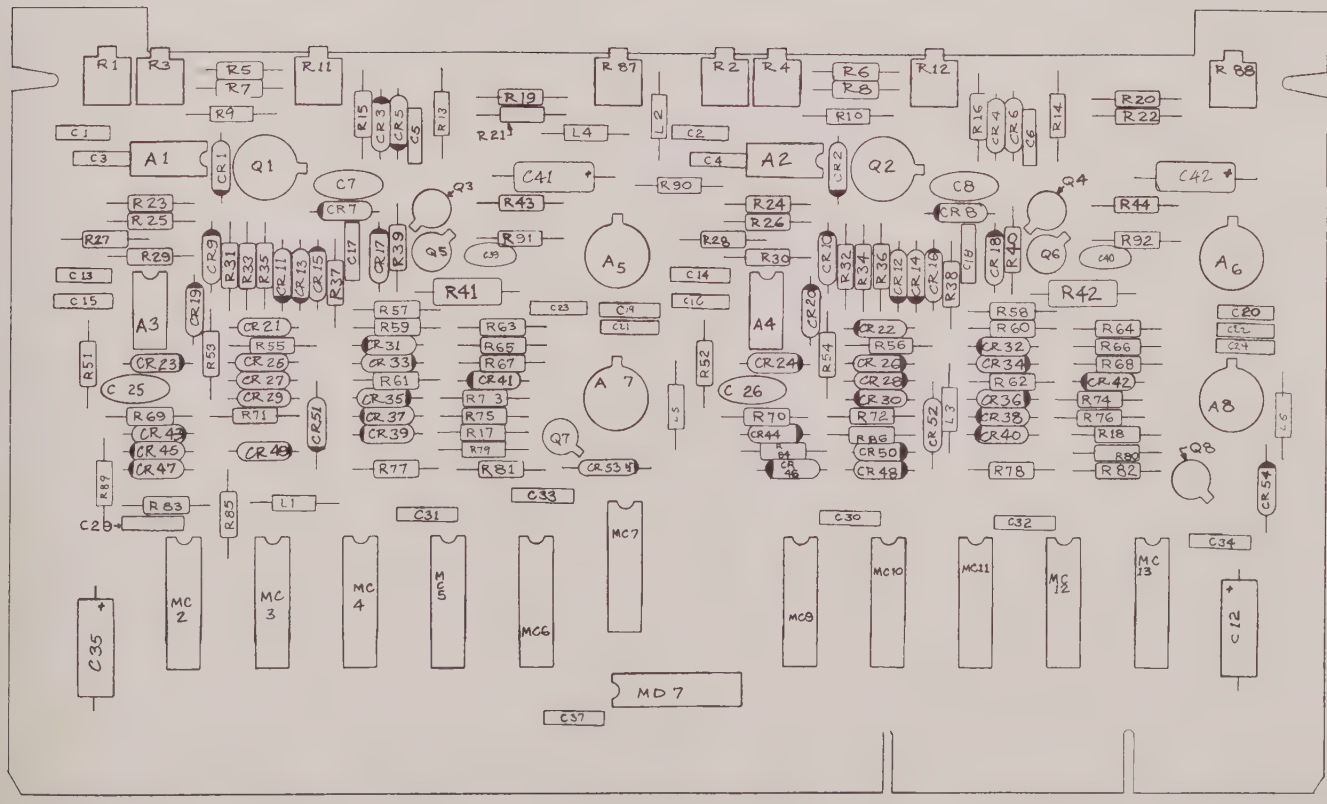




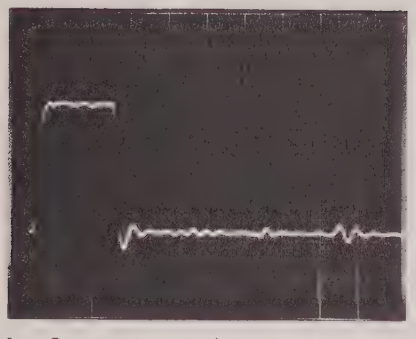


NOTE:

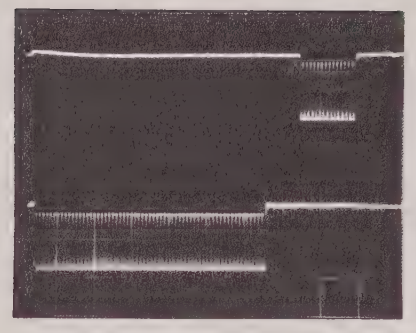
1. ⏚ AND ⏚ DENOTE ELECTRICALLY SEPARATE GROUND PLANES. ⏚ DENOTES DIGITAL GROUND PLANE.
2. BOARD PIN MNEMONICS IN PARENTHESES APPLY WHEN BOARD IS PLUGGED INTO ITS REARMOST CONNECTOR ON MOTHERBOARD.



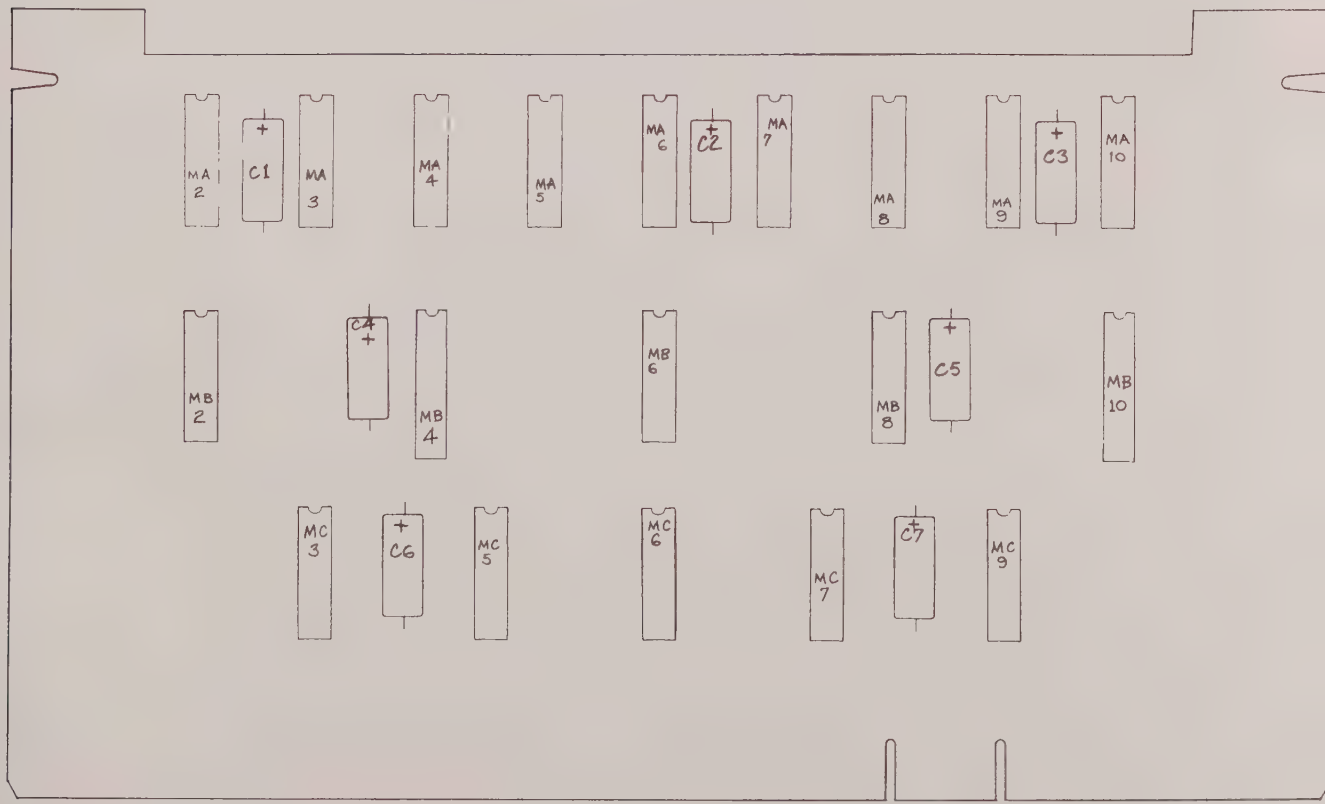
A/D Converter
-93A-

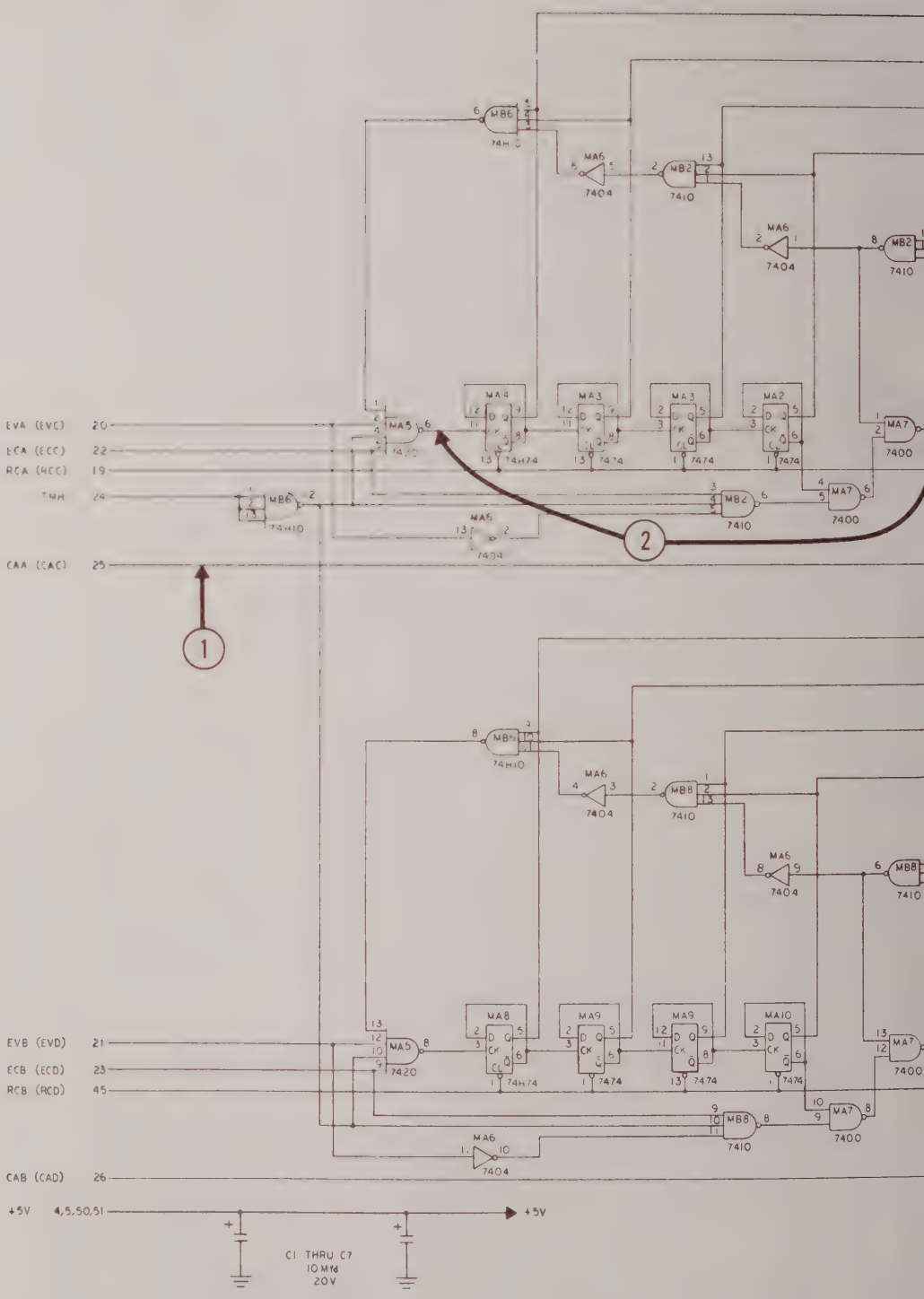


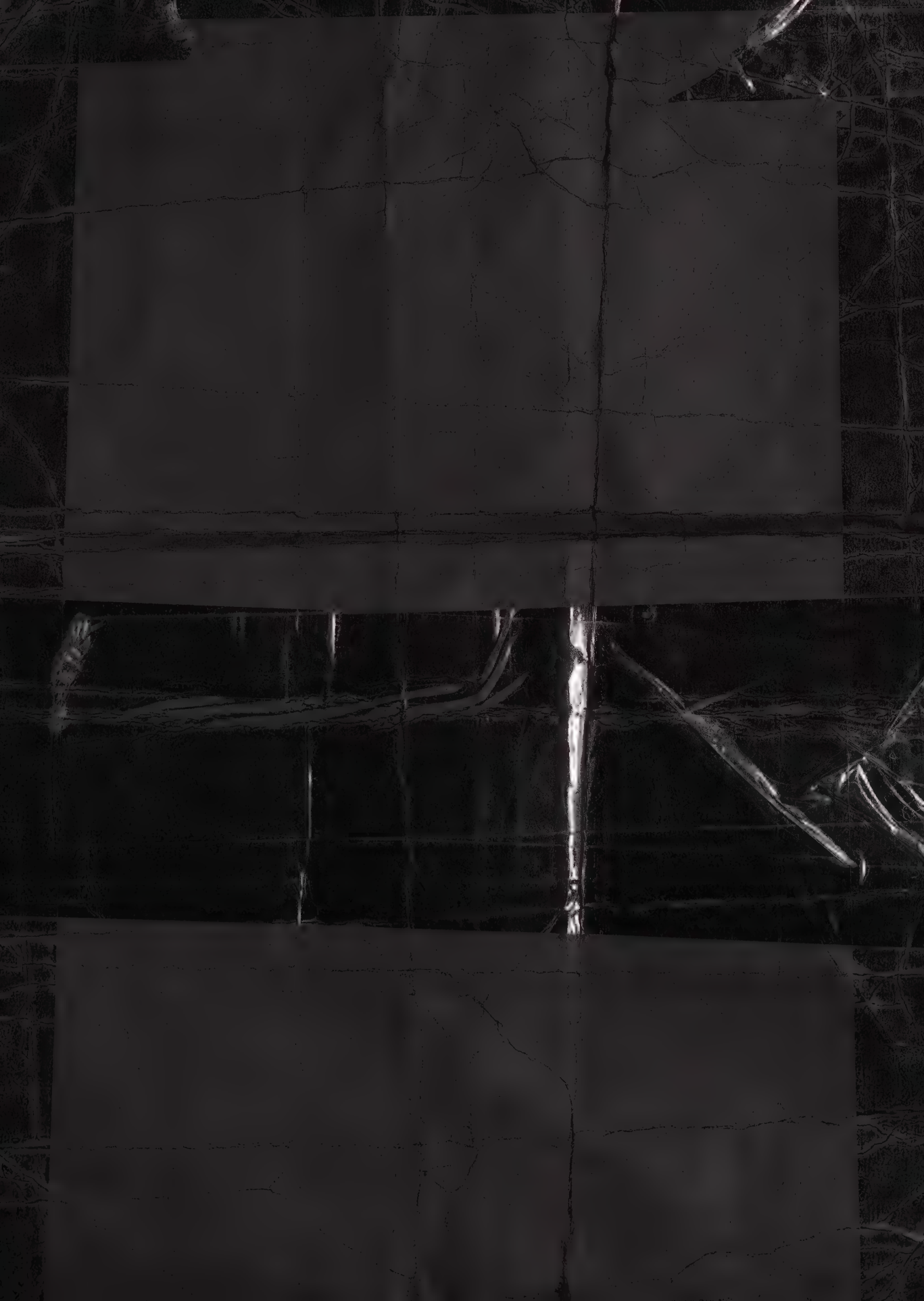
1. Scope: Vert. 1 v/div, Horz. .1 μsec/div.
   Trigger: Int + slope.
   1015: Pre trig record, sample interval .01 msec, unit armed, offset full CCW.

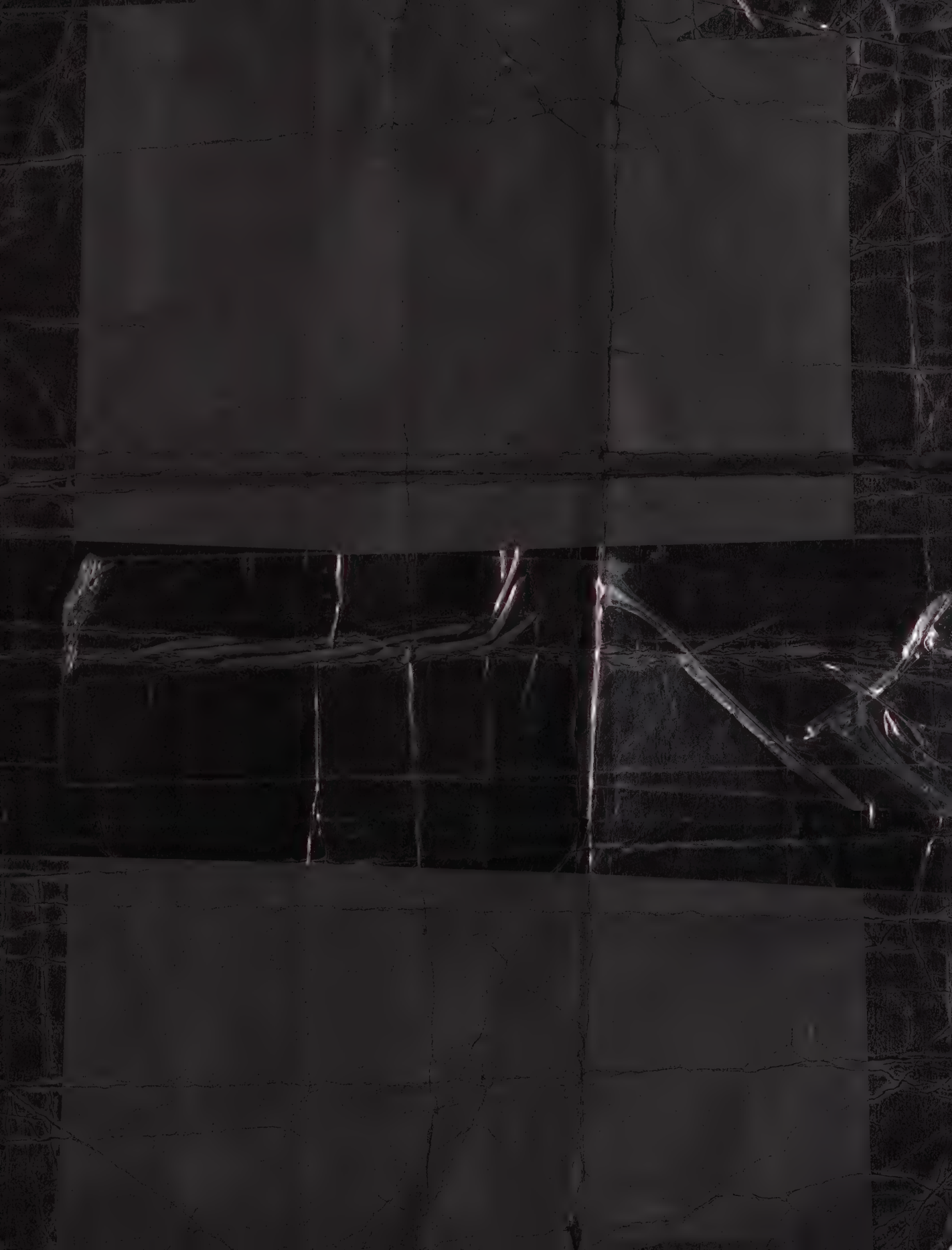


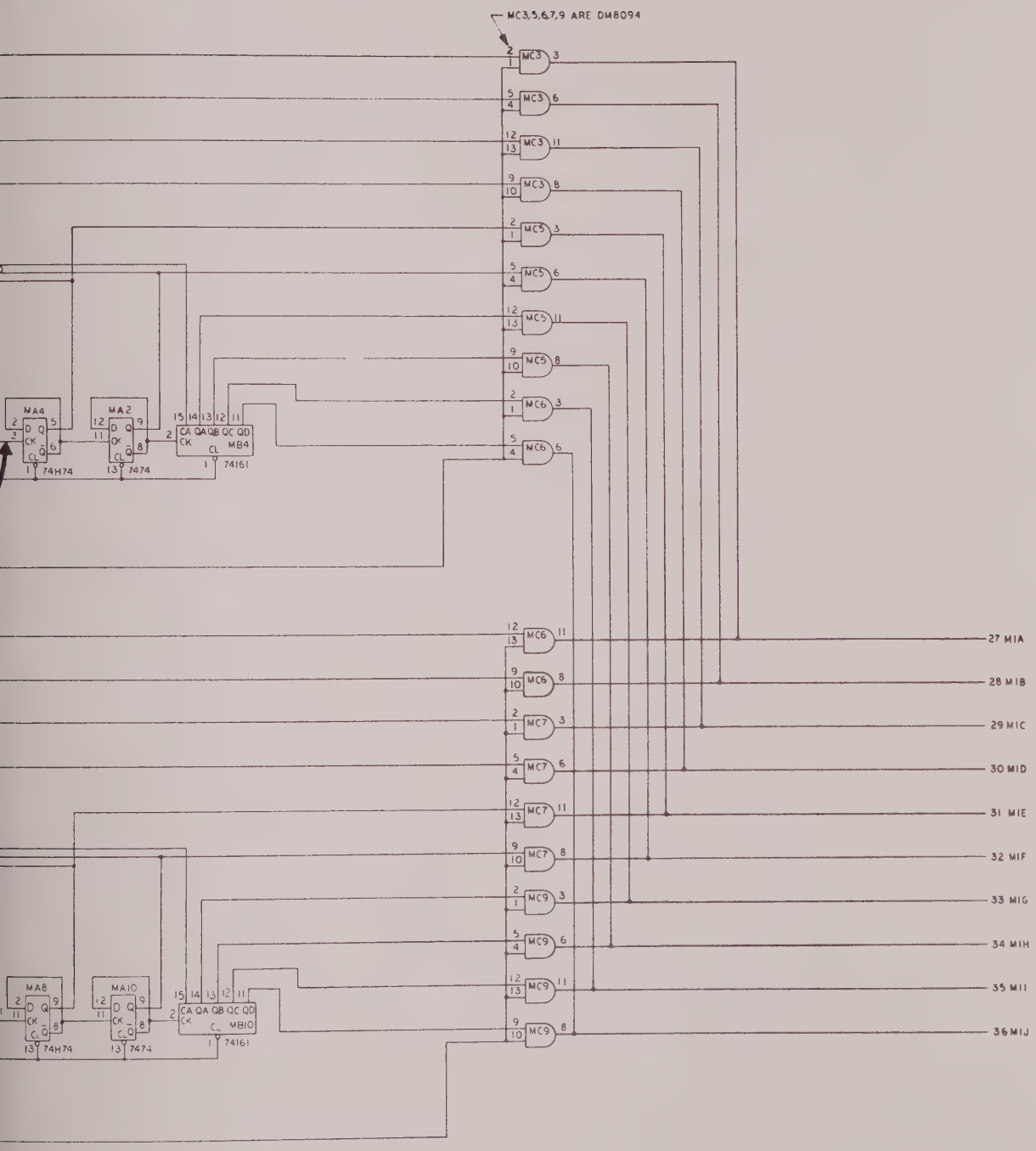
2. Scope: Vert. CH 1 & 2 2 v/div, Horz. .5μsec/div.
   Trigger: Ext on "RCA."
   1015: Pre trig record, sample interval .01 msec, unit armed, offset full CCW.



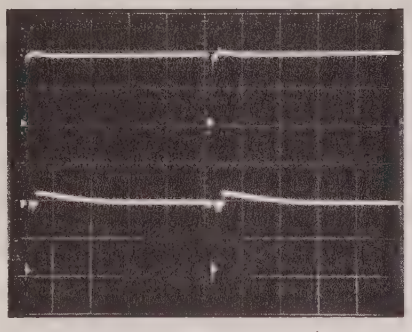

EVA (EVC) 20
ECA (ECC) 22
RCA (RCC) 19
TMH 24
CAA (CAC) 25
EVB (EVD) 21
ECB (ECD) 23
RCB (RCD) 45
CAB (CAD) 26
+5V 4,5,50,51
+5V
C1 THRU C7
10 Mfd
20V
1
2
MA5
MA6
MA7
MA8
MA9
MA10
MB2
MB6
MB8
7400
7404
7410
7420
74H10
74H74
7474



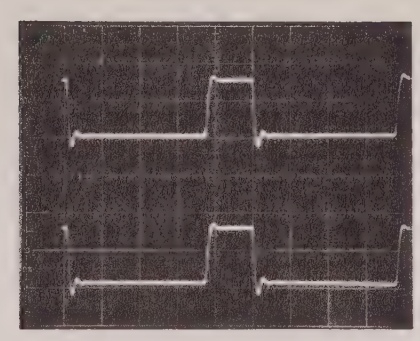




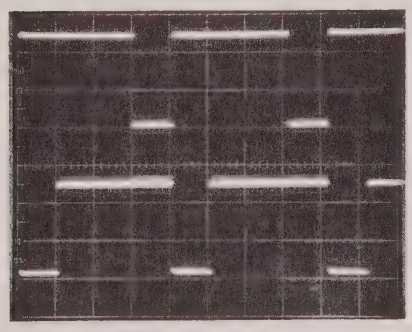
ADC Counter Multiplex



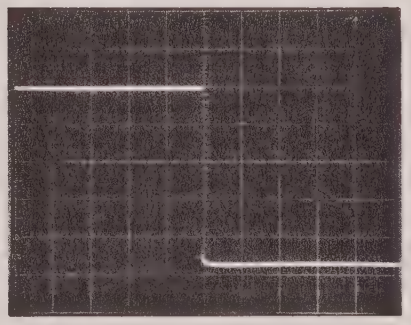
1. Scope: Vert. CH 1 & 2 2 v/div, Horz. 2μsec/div.
Trigger: Int CH 1 – slope.
1015: Pre trig record, sample interval .01msec, unit armed.



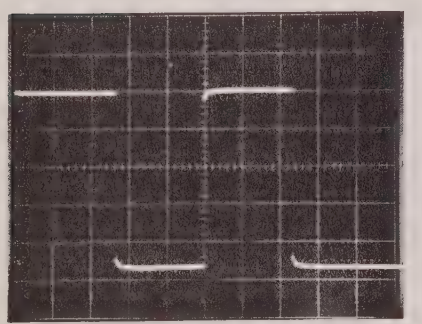
2. Scope: Vert. CH 1 & 2 2 v/div, Horz. .2μsec/div.
Trigger: Int CH 1 – slope.
1015: In display mode.



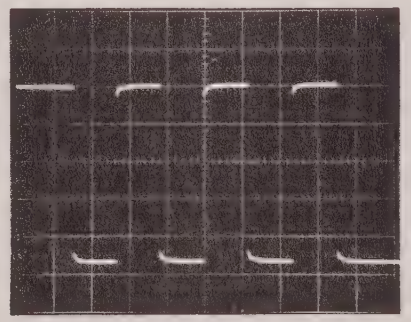
3. Scope: Vert. CH 1 & 2 2 v/div, Horz. 1msec/div.
Trigger: Int CH 1 Pos Slope.
1015: In display mode.



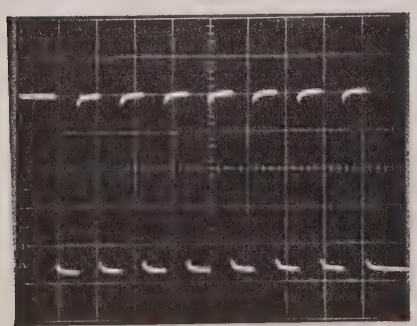
4. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Ext on "ADDR1" + slope.
1015: Display mode 25 Hz triangle wave full scale sample interval .01 ms trig on gen. sync.



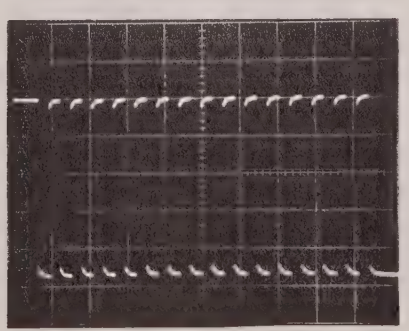
5. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4
1015: Same as 4



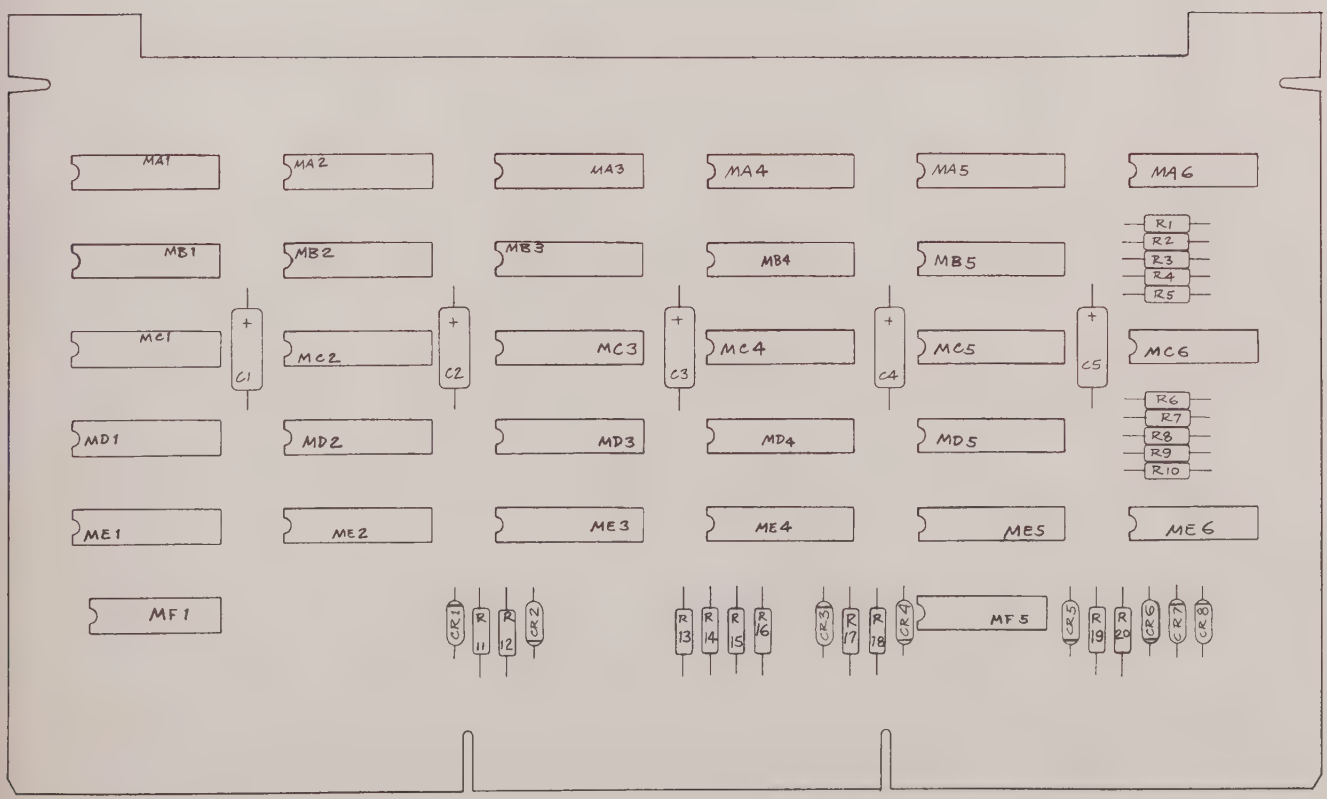
6. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.

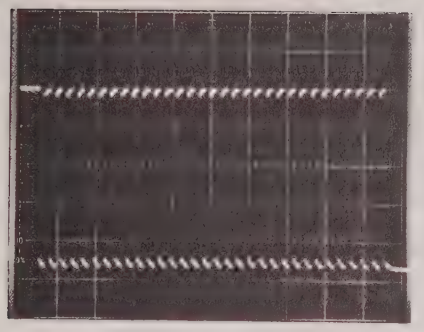


7. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.

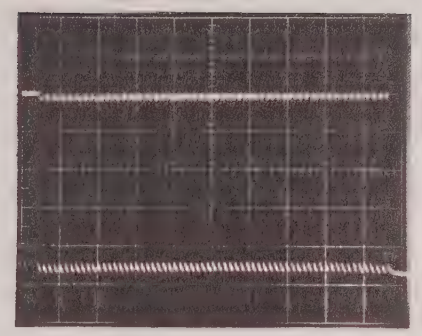


8. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.

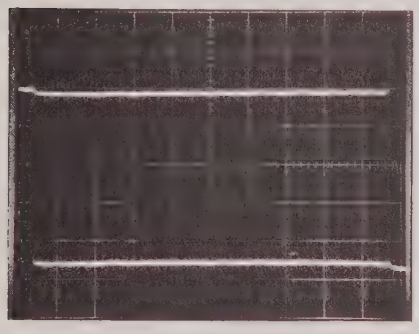

MA1
MA2
MA3
MA4
MA5
MA6
MB1
MB2
MB3
MB4
MB5
MC1
MC2
MC3
MC4
MC5
MC6
MD1
MD2
MD3
MD4
MD5
ME1
ME2
ME3
ME4
ME5
ME6
MF1
MF5
C1
C2
C3
C4
C5
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8



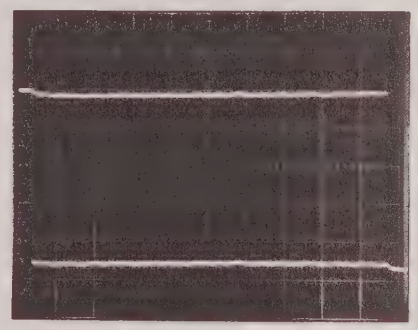
9. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.



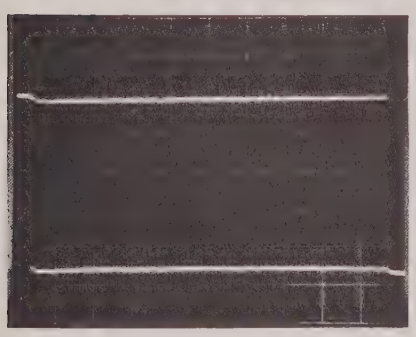
10. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.



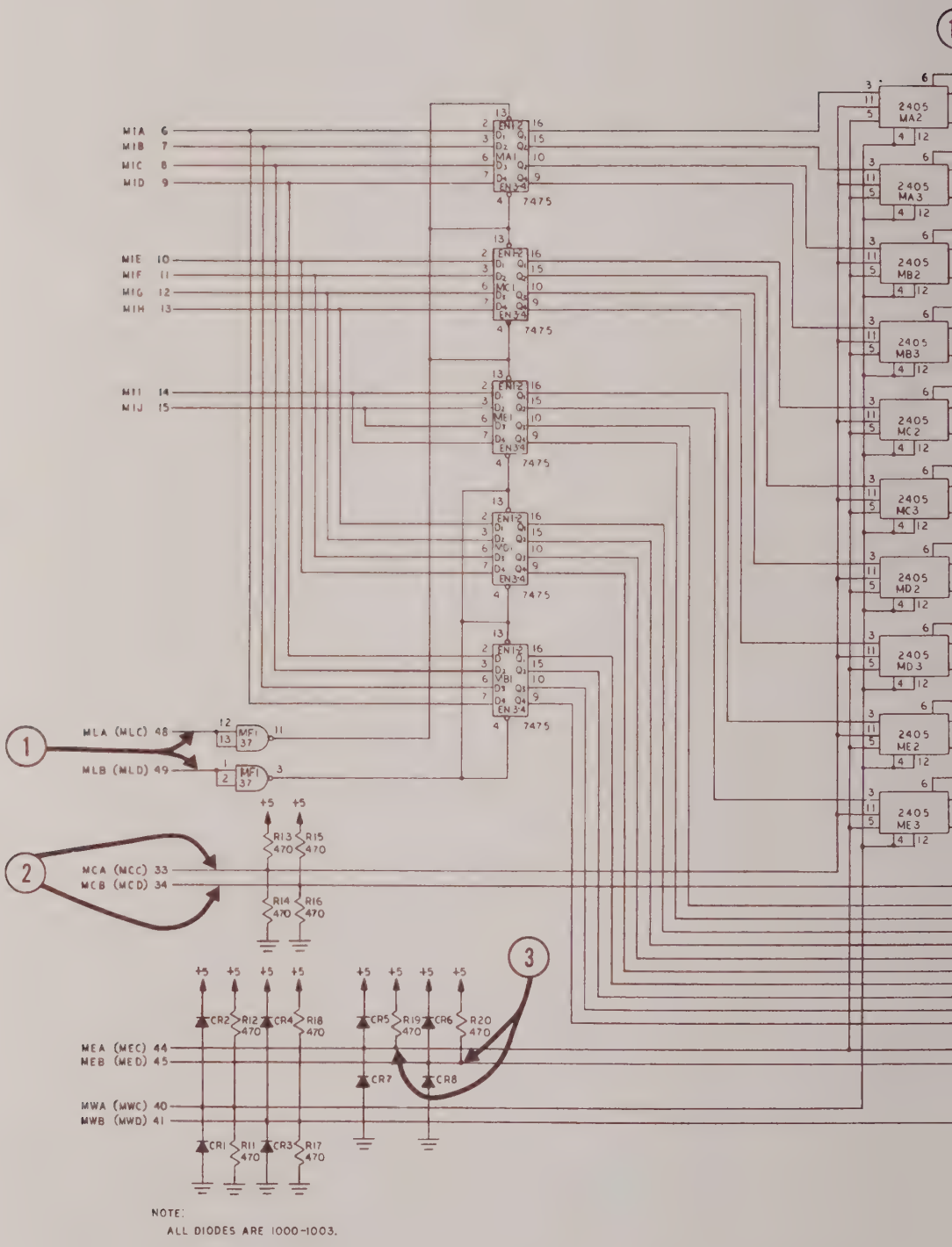
11. Scope: 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.



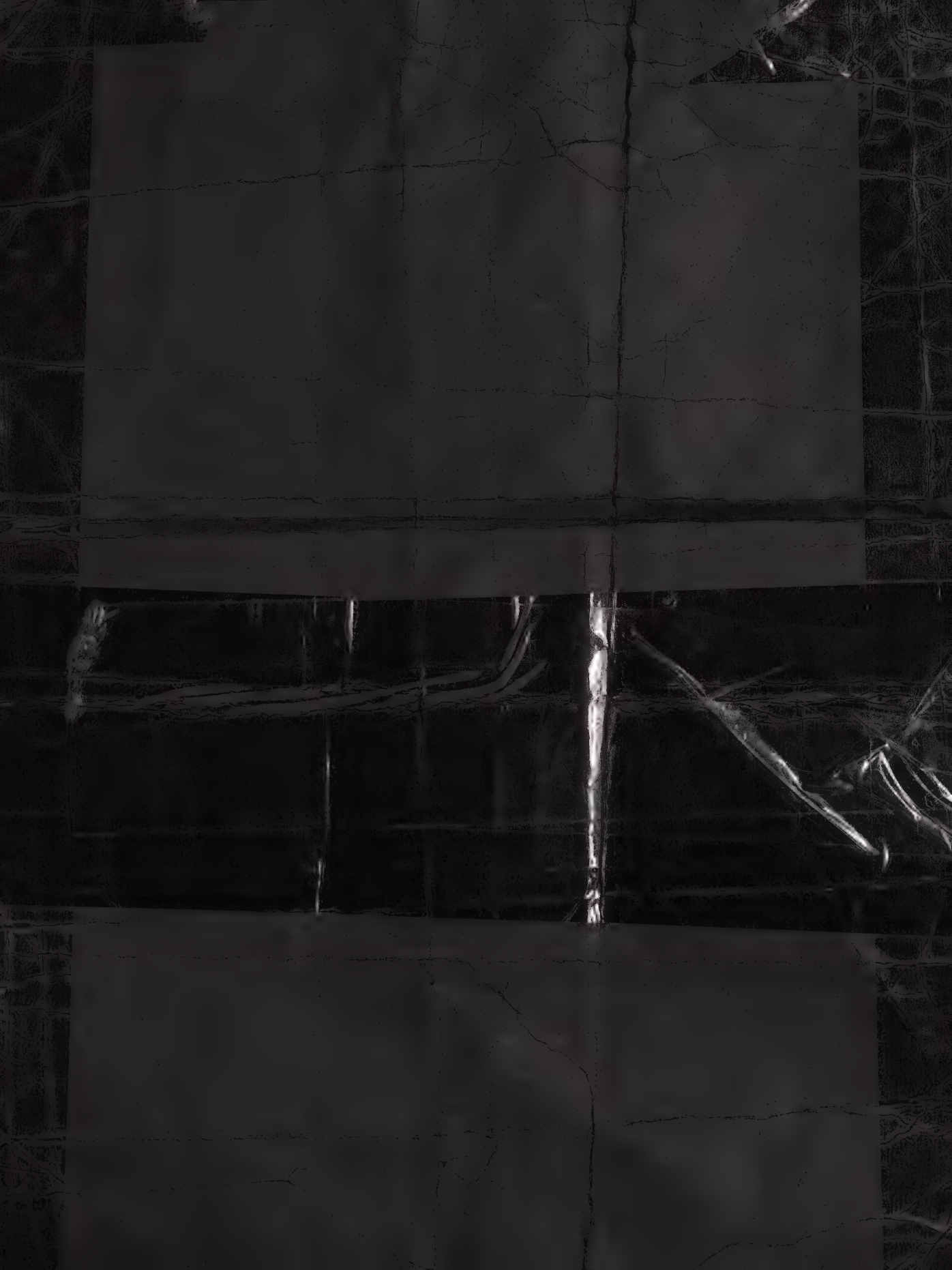
12. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.

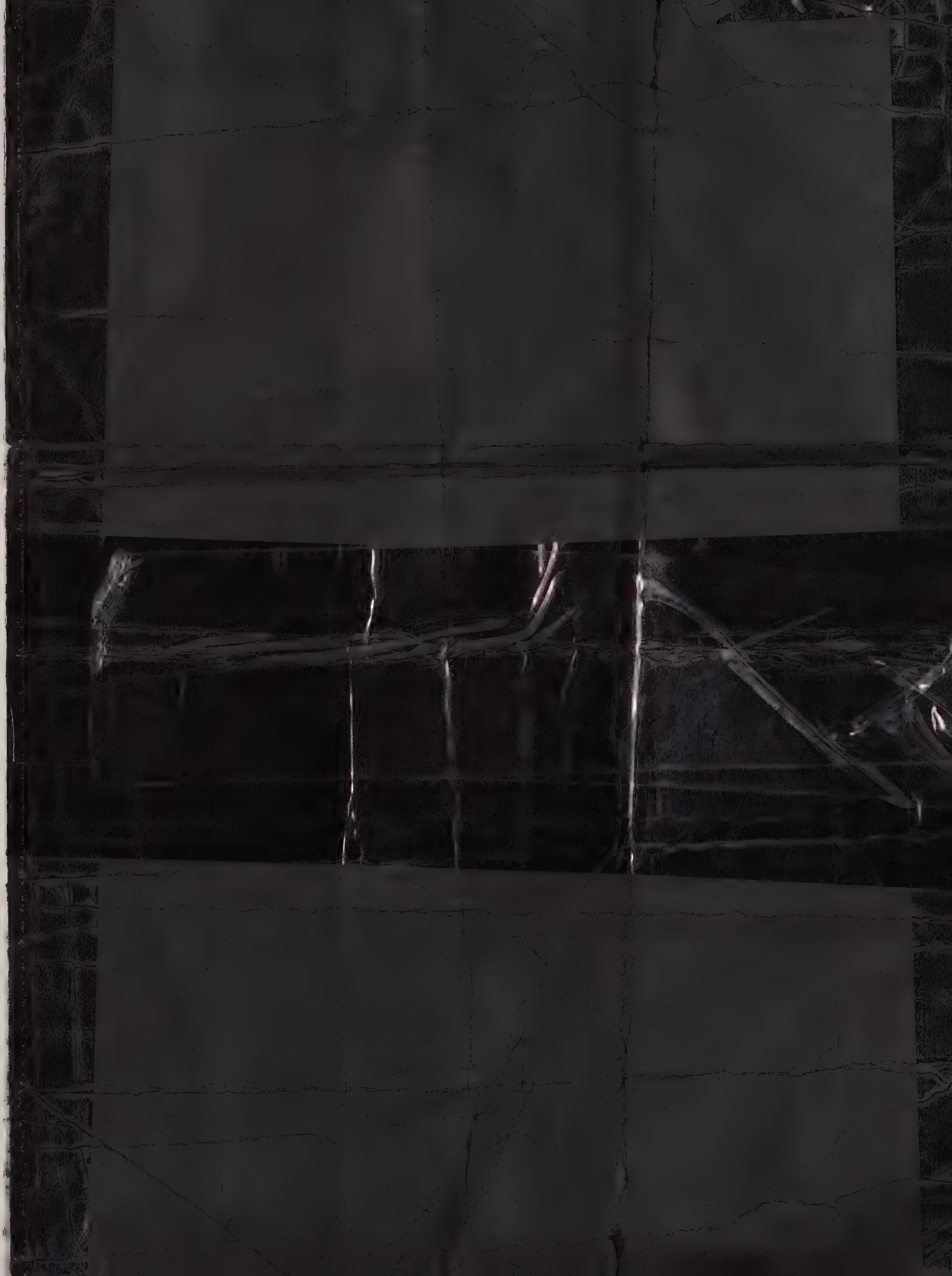


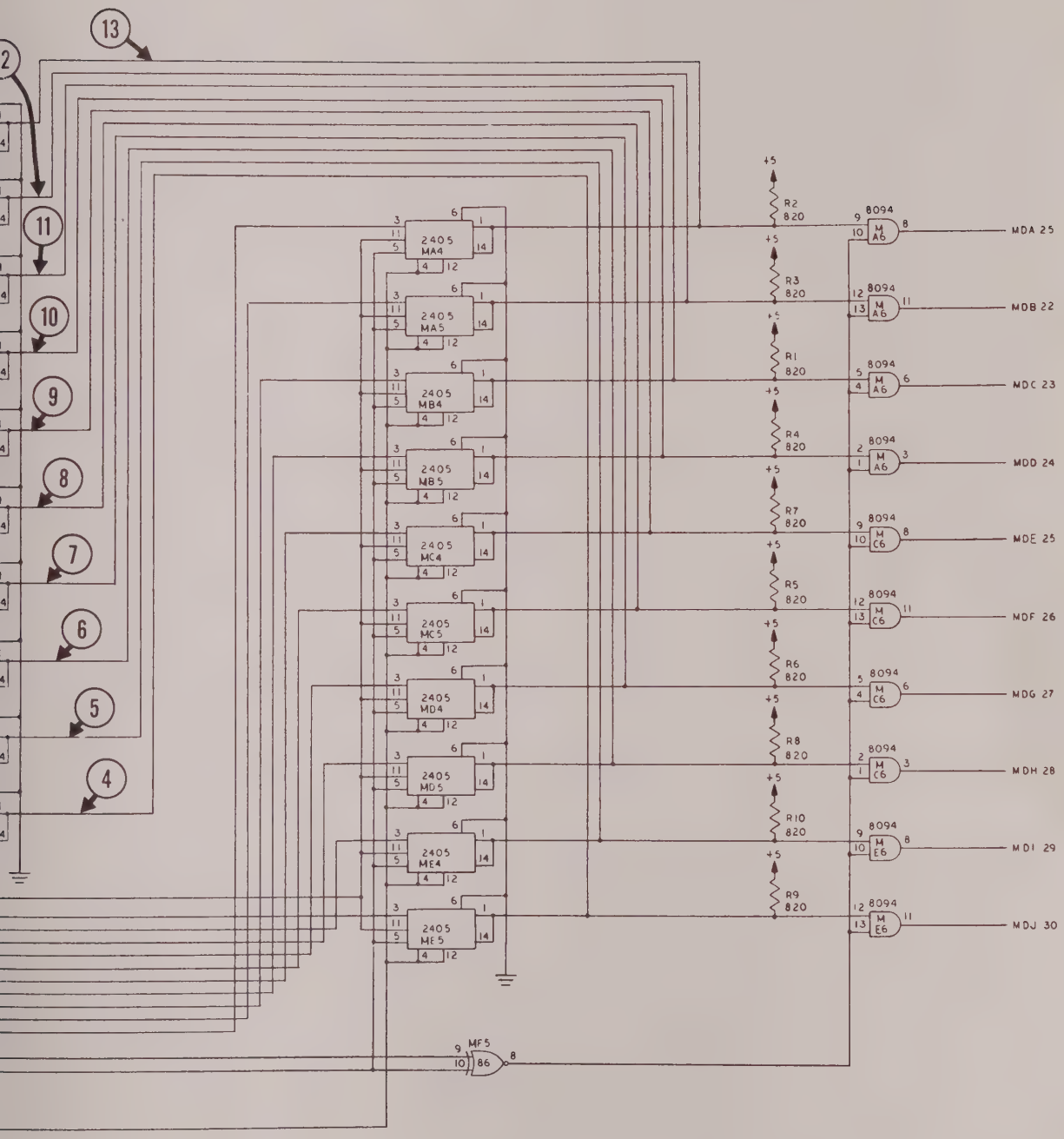
13. Scope: Vert. 1 v/div, Horz. .1 msec/div.
Trigger: Same as 4.
1015: Same as 4.

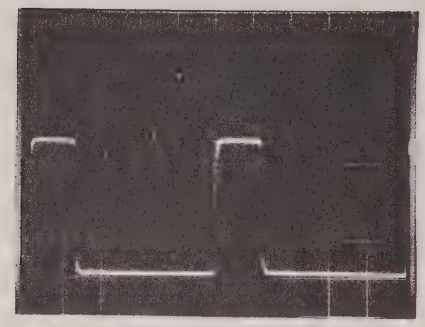


NOTE:
ALL DIODES ARE 1000-1003.

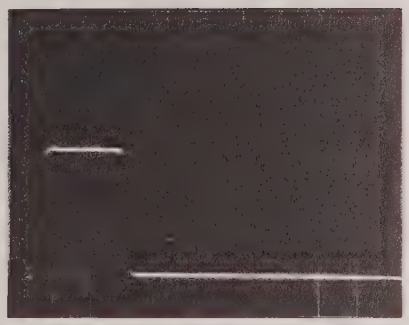




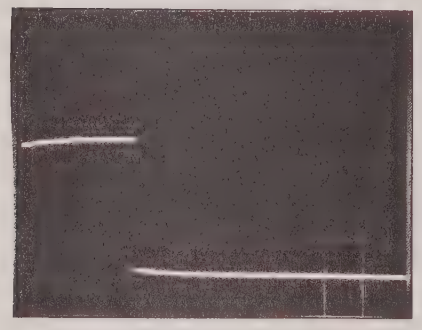

13
12
11
10
9
8
7
6
5
4
+5
R2 820
R3 820
R1 820
R4 820
R7 820
R5 820
R6 820
R8 820
R10 820
R9 820
2405 MA4
2405 MA5
2405 MB4
2405 MB5
2405 MC4
2405 MC5
2405 MD4
2405 MD5
2405 ME4
2405 ME5
8094 M A6
8094 M A6
8094 M A6
8094 M A6
8094 M C6
8094 M C6
8094 M C6
8094 M C6
8094 M E6
8094 M E6
MDA 25
MDB 22
MDC 23
MDD 24
MDE 25
MDF 26
MDG 27
MDH 28
MDI 29
MDJ 30
MF5



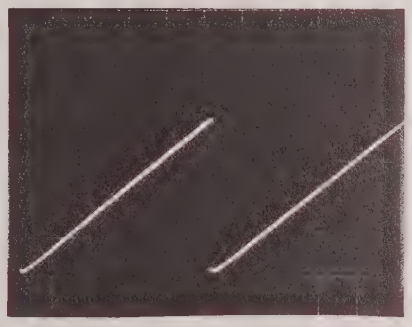
1. Scope: Vert. 1 v/div, Horz. .2 μsec/div.
Trigger: Int + slope.
1015: In display.



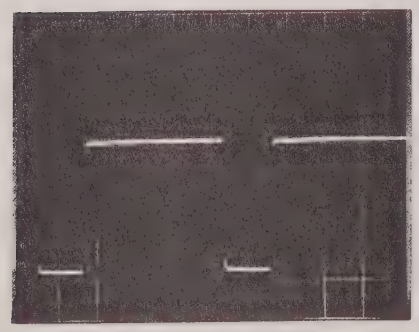
2. Scope: Vert. 1 v/div, Horz. .1 μsec/div.
Trigger: Int + slope.
1015: In display.



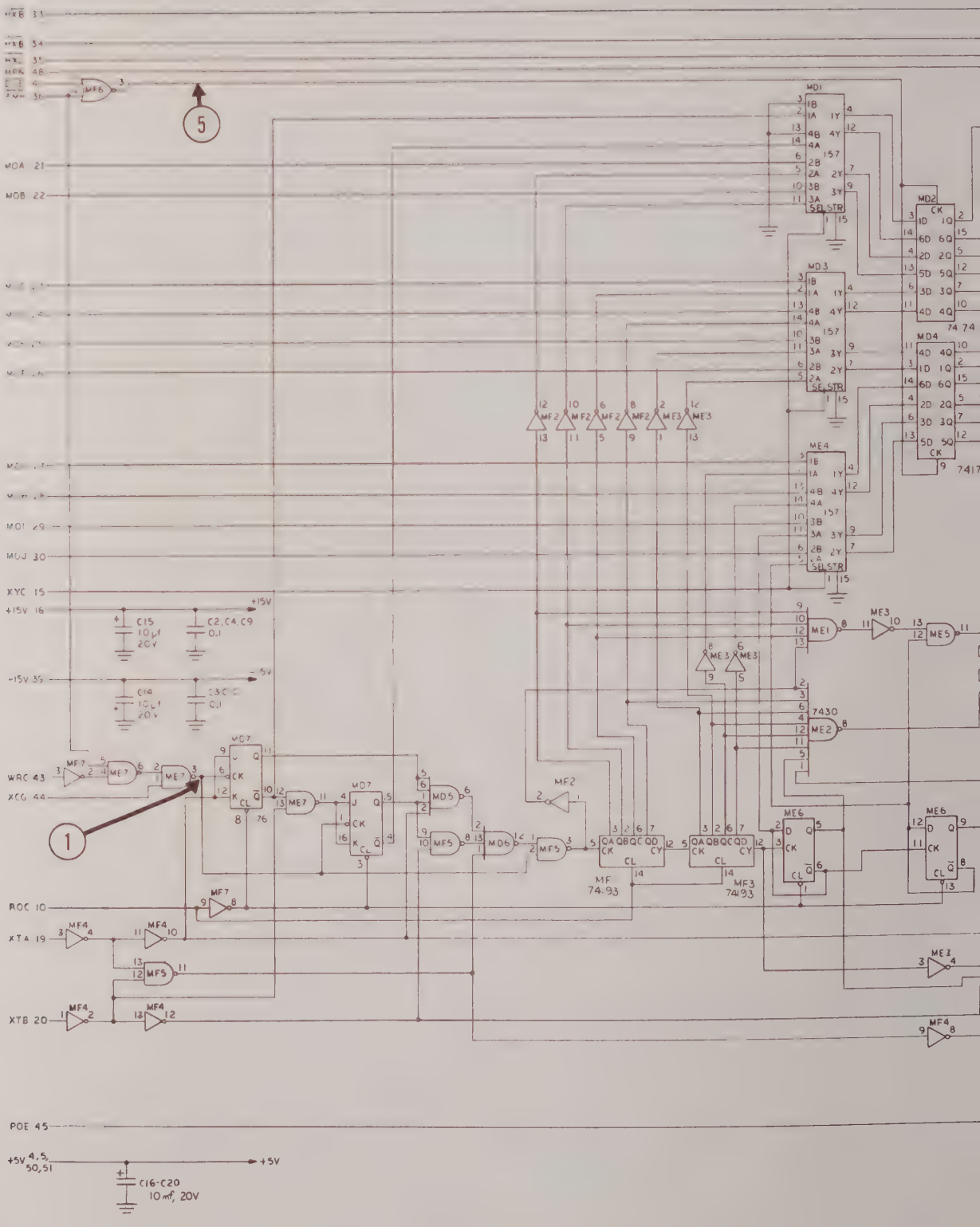
3. Scope: Vert; 1 v/div, Horz. 5 μsec/div.
Trigger: Int + slope.
1015: In display. Pulse rate 1msec.

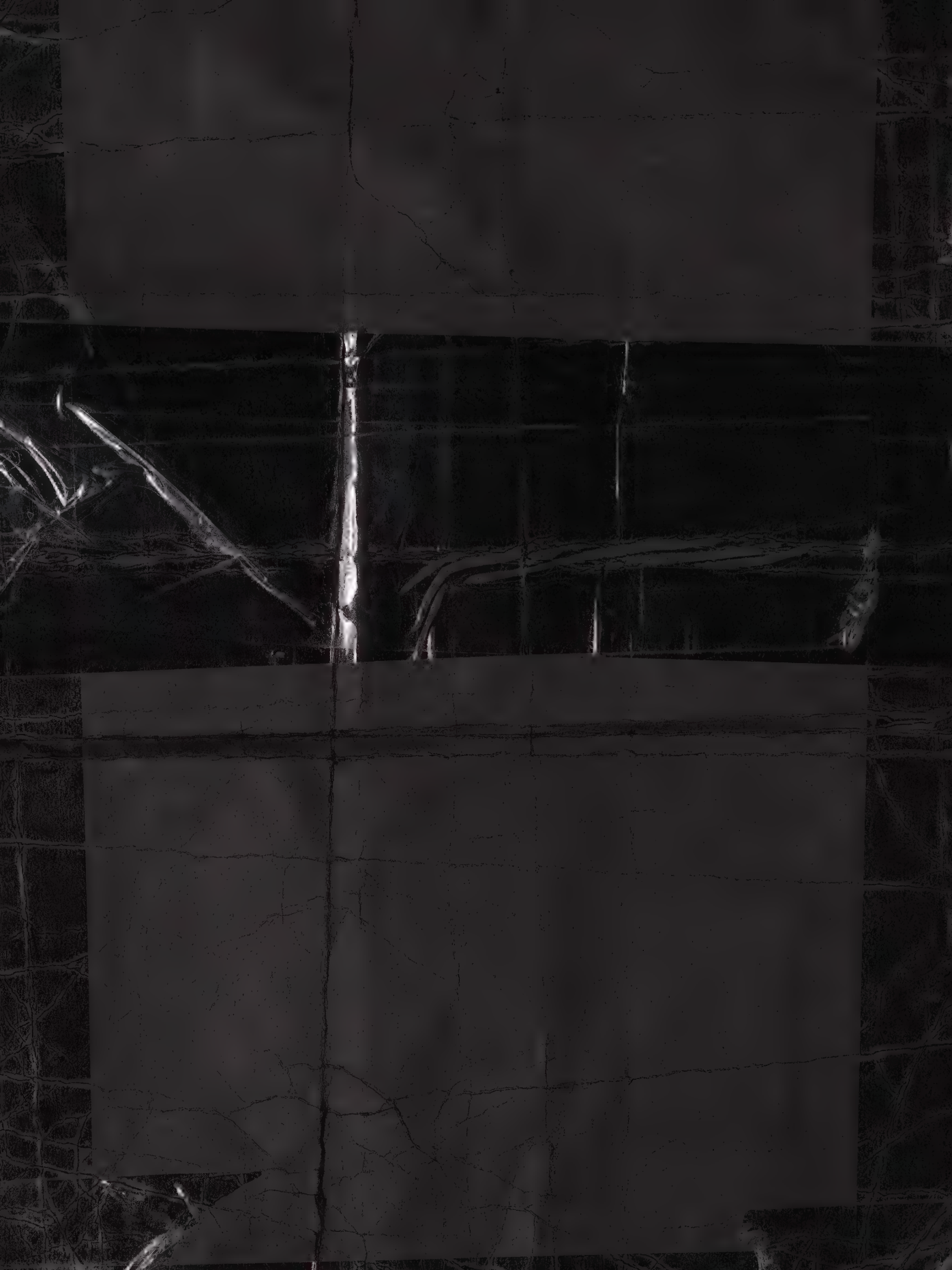


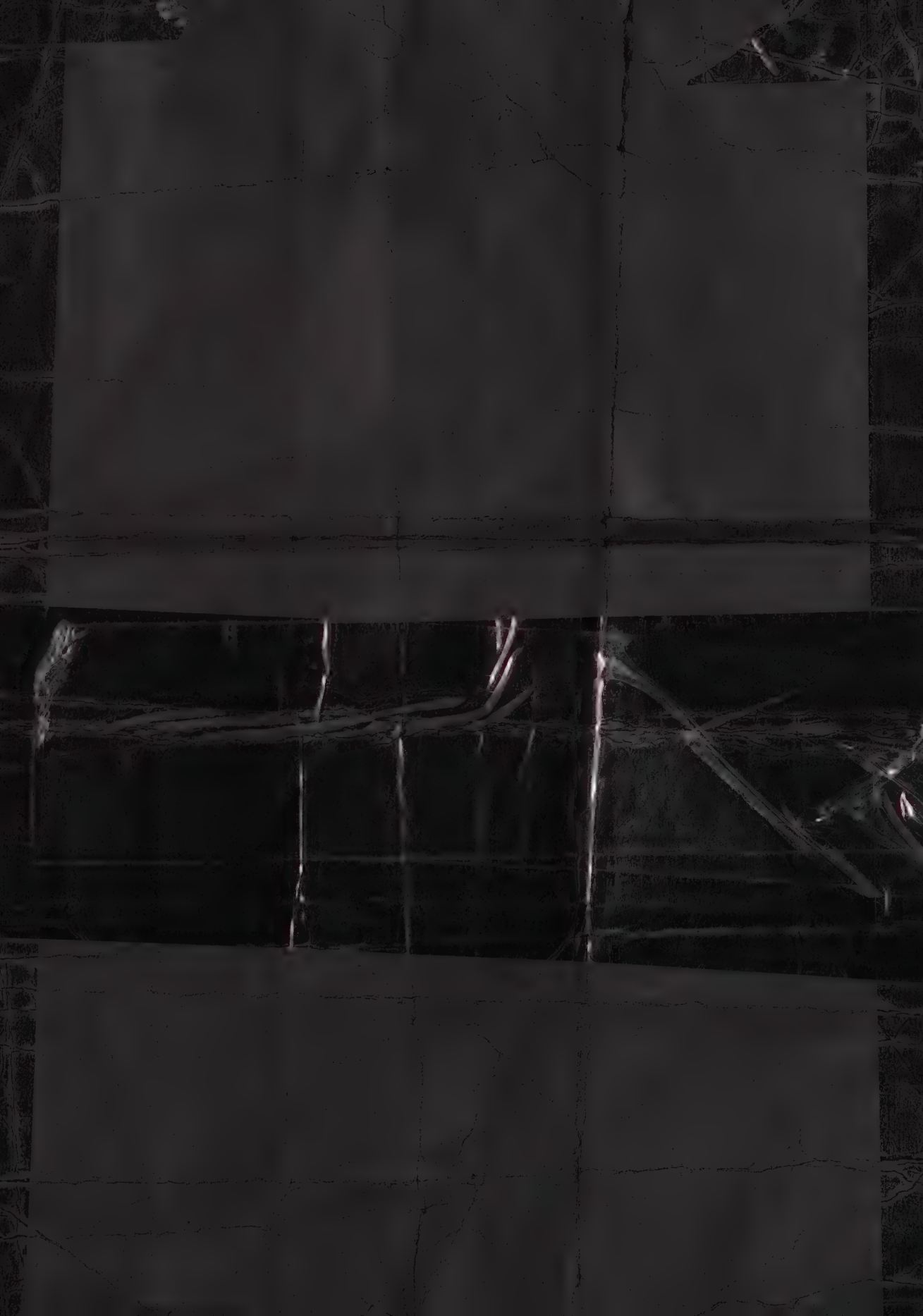
4. Scope: Vert. .5 v/div, Horz. .2 msec/div.
Trigger: Int – slope.
1015: In display.

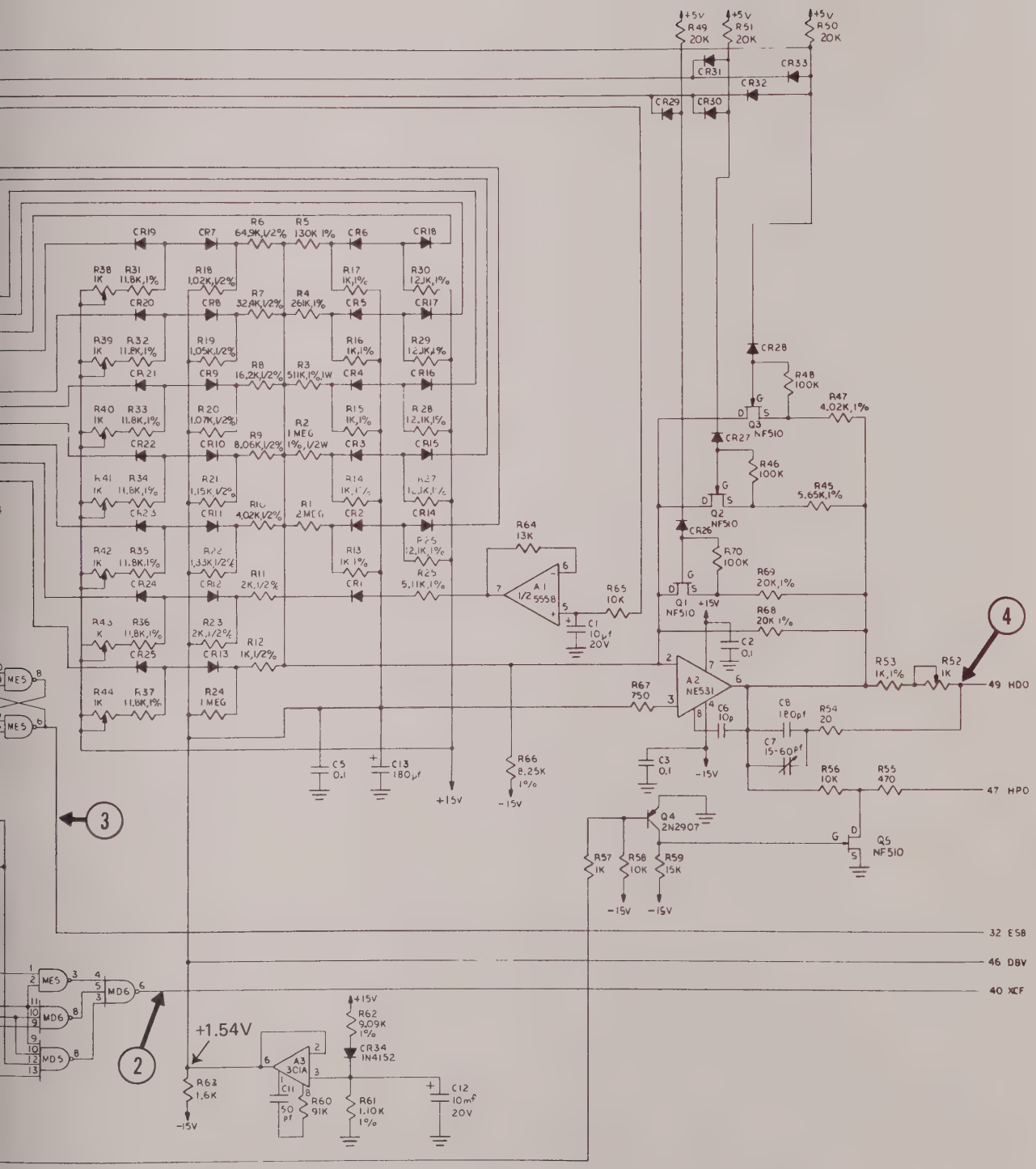


5. Scope: Vert. 1 v/div, Horz. .2 μsec/div.
Trigger: Int – slope.
1015: In display.

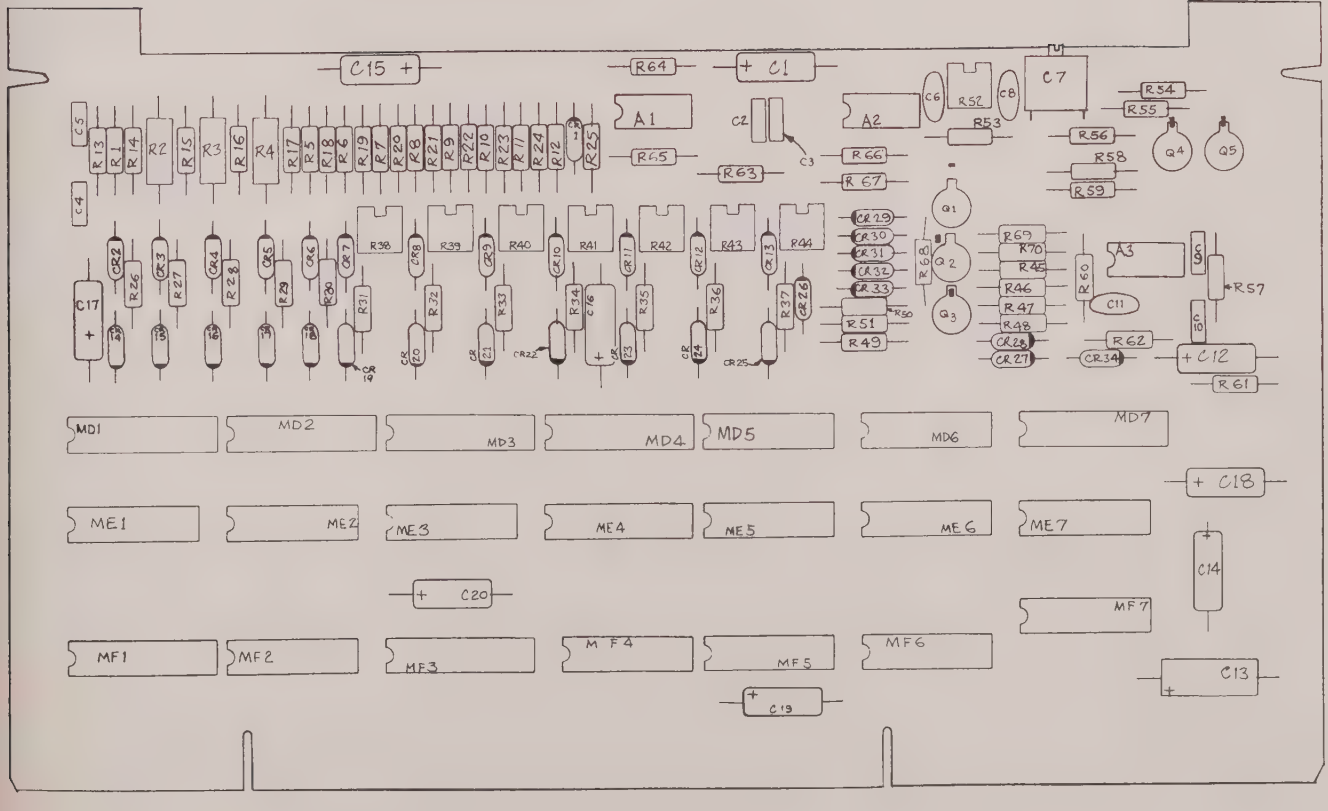

MXB 33
MXB 34
MOA 21
MOB 22
XYC 15
+15V 16
-15V 35
WRC 43
XCG 44
POC 10
XTA 19
XTB 20
POE 45
+5V 4,5, 50,51
+5V
C16-C20 10 mf, 20V
C15 10 µf 20V
C2,C4,C9 0.1
C14 10 µf 20V
C3,C5,C8 0.1
MD1
MD2
MD3
MD4
ME1
ME2
ME3
ME4
ME5
ME6
ME7
MF2
MF3
MF4
MF5
MF6
MF7
MD5
MD6
MD7
7430
74 74
7417
MF 74.93
MF3 74193
SEL STR
5
1



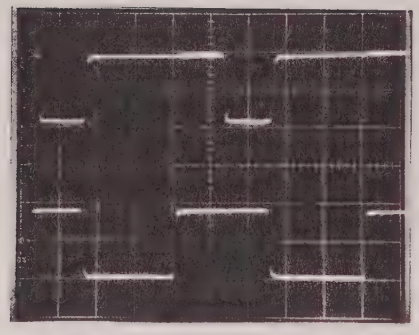



+5V
R49 20K
R51 20K
R50 20K
CR31
CR33
CR32
CR29
CR30
CR19
CR7
R6 64.9K,1/2%
R5 130K 1%
CR6
CR18
R38 1K
R31 11.8K,1%
R18 1.02K,1/2%
R17 1K,1%
R30 12.1K,1%
CR20
CR8
R7 32.4K,1/2%
R4 26.1K,1%
CR5
CR17
R39 1K
R32 11.8K,1%
R19 1.05K,1/2%
R16 1K,1%
R29 12.1K,1%
CR21
CR9
R8 16.2K,1/2%
R3 511K,1%,1W
CR4
CR16
R40 1K
R33 11.8K,1%
R20 1.07K,1/2%
R15 1K,1%
R28 12.1K,1%
CR22
CR10
R9 8.06K,1/2%
R2 1 MEG 1%,1/2W
CR3
CR15
R41 1K
R34 11.8K,1%
R21 1.15K,1/2%
R14 1K,1%
R27 12.1K,1%
CR23
CR11
R10 4.02K,1/2%
R1 2 MEG
CR2
CR14
R42 1K
R35 11.8K,1%
R22 1.33K,1/2%
R13 1K 1%
R26 12.1K,1%
CR24
CR12
R11 2K,1/2%
CR1
R25 5.11K,1%
R43 1K
R36 11.8K,1%
R23 2K,1/2%
CR25
CR13
R12 1K,1/2%
R44 1K
R37 11.8K,1%
R24 1 MEG
CR28
R48 100K
R47 4.02K,1%
Q3 NF510
CR27
R46 100K
R45 5.65K,1%
Q2 NF510
CR26
R70 100K
R69 20K,1%
Q1 NF510
+15V
R68 20K 1%
R64 13K
A1 1/2 5558
R65 10K
C1 10µf 20V
C2 0.1
R67 750
A2 NE531
C6 10p
CB 180pf
R54 20
C7 15-60pf
R53 1K,1%
R52 1K
49 HDO
C5 0.1
C13 180µf
+15V
-15V
R66 8.25K 1%
C3 0.1
-15V
R56 10K
R55 470
47 HPO
Q4 2N2907
Q5 NF510
R57 1K
R58 10K
R59 15K
-15V
-15V
32 ESB
46 DBV
40 XCF
MES
MES
MD6
MD6
MD5
+1.54V
R63 1.6K
-15V
A3 3C1A
C11 50 pf
R60 91K
+15V
R62 9.09K 1%
CR34 1N4152
R61 1.10K 1%
C12 10mf 20V
2
3
4

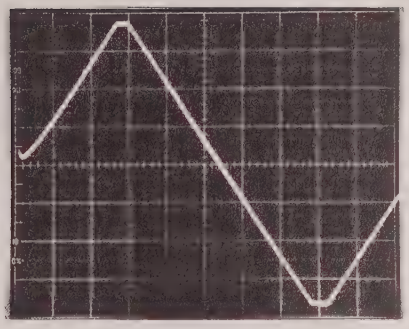
X Output D/A



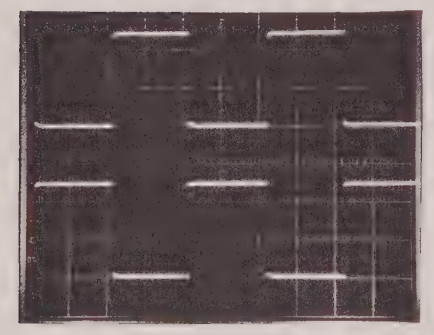
X Output D/A
-97A-



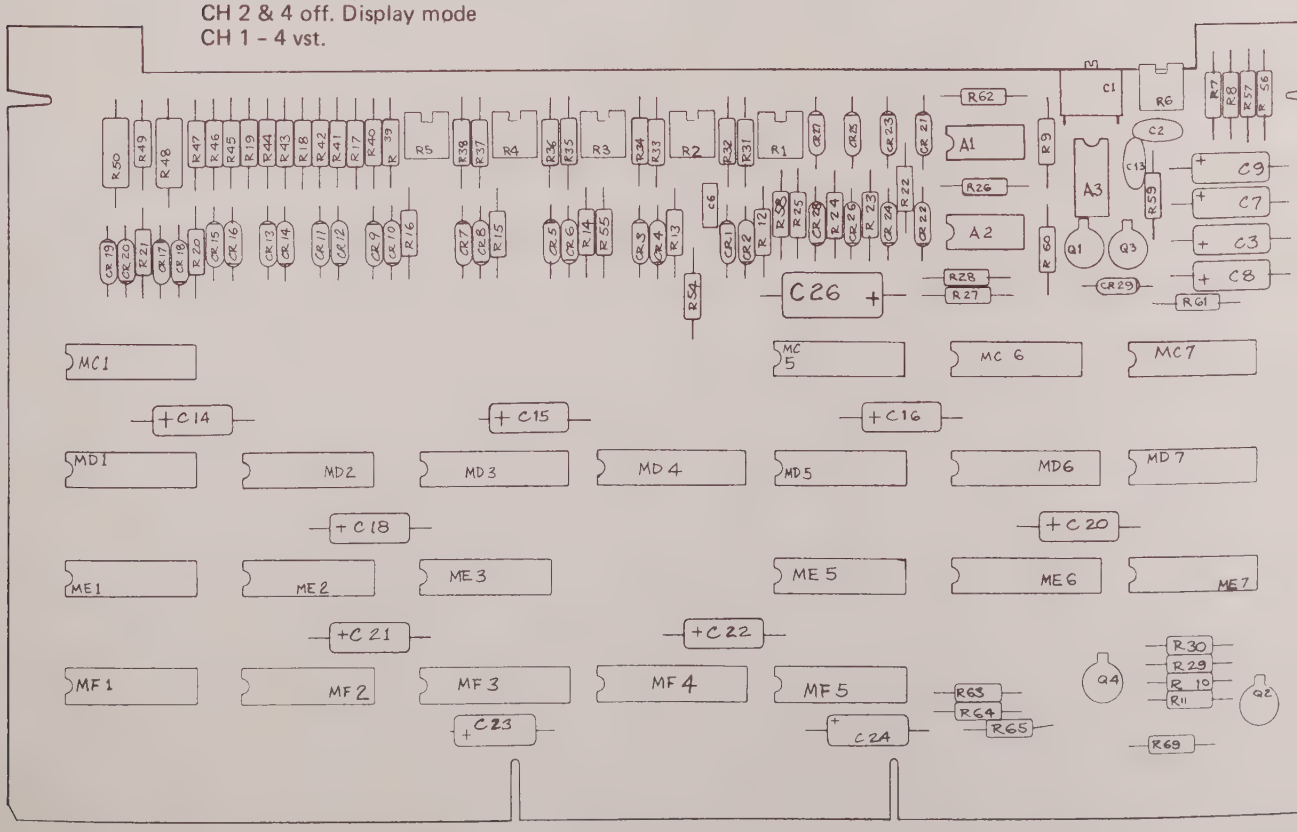
1. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. .2μsec/div.
   Trigger: Int Chan 1 — slope.
   1015: In display.

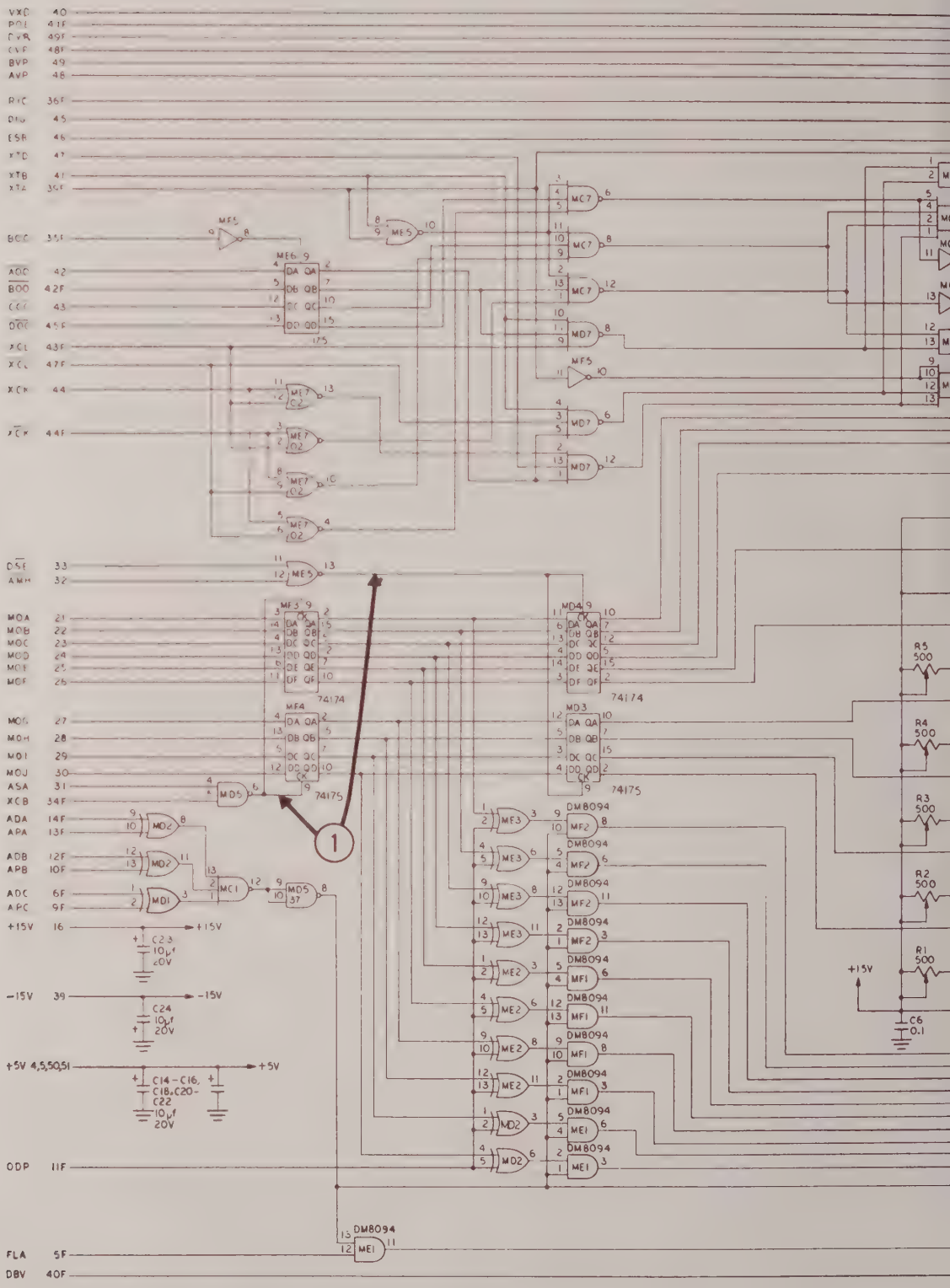


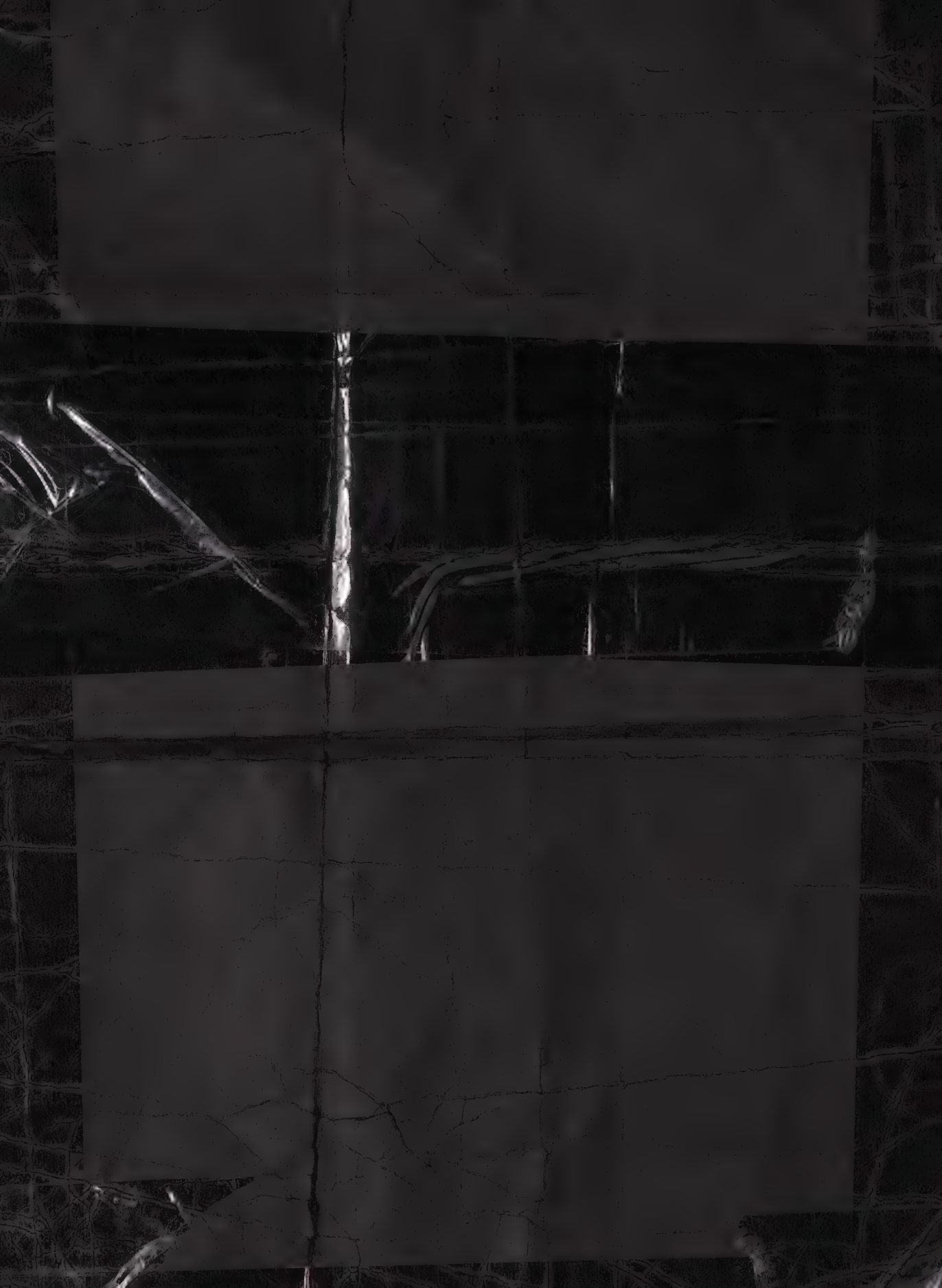
2. Scope: Vert. .2 v/div, Horz. .1
   msec/div.
   Trigger: Int — slope.
   1015: In display 100 Hz triangle.
   Stored in memory Ch 1, Ch 2;
   3, 4 off.

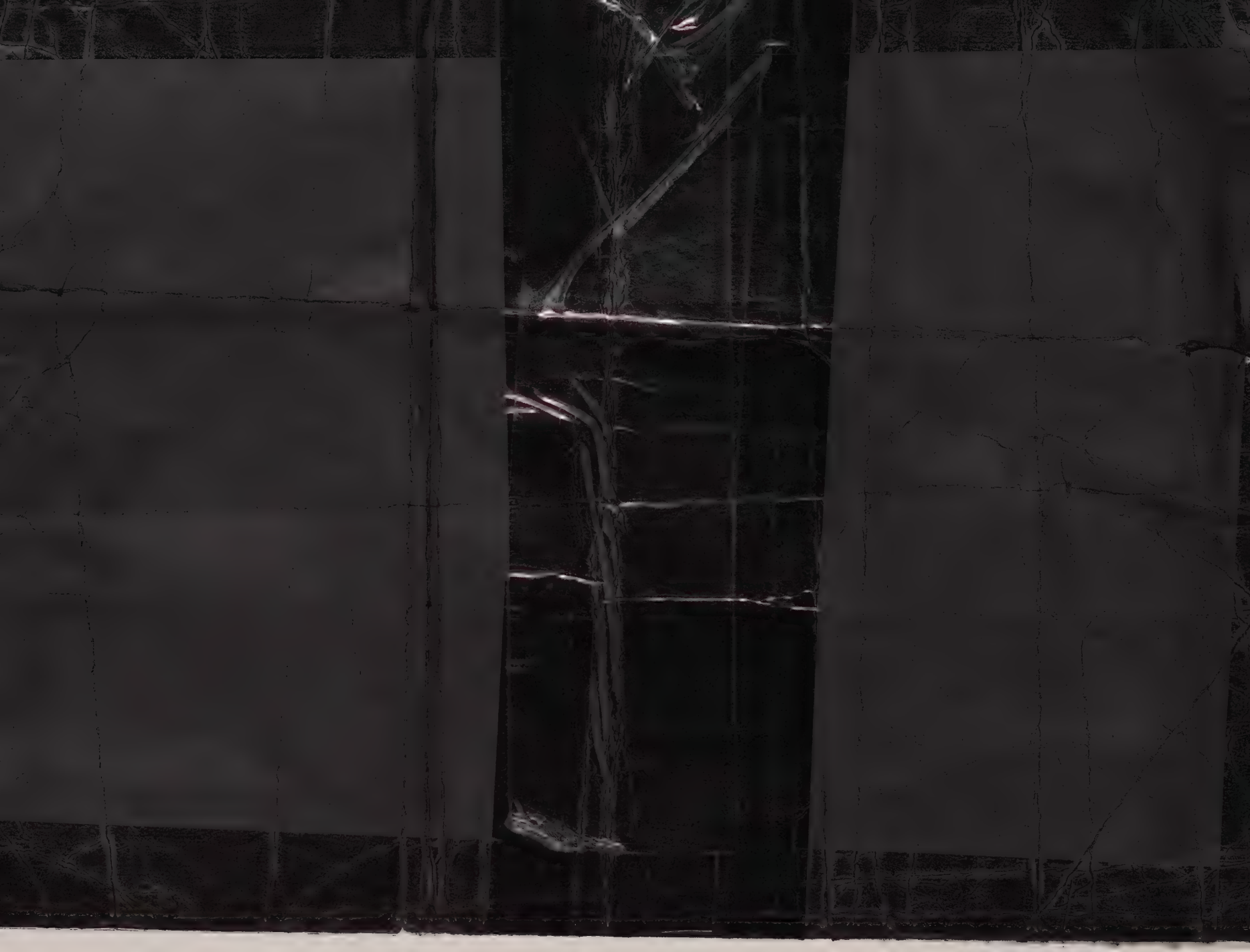


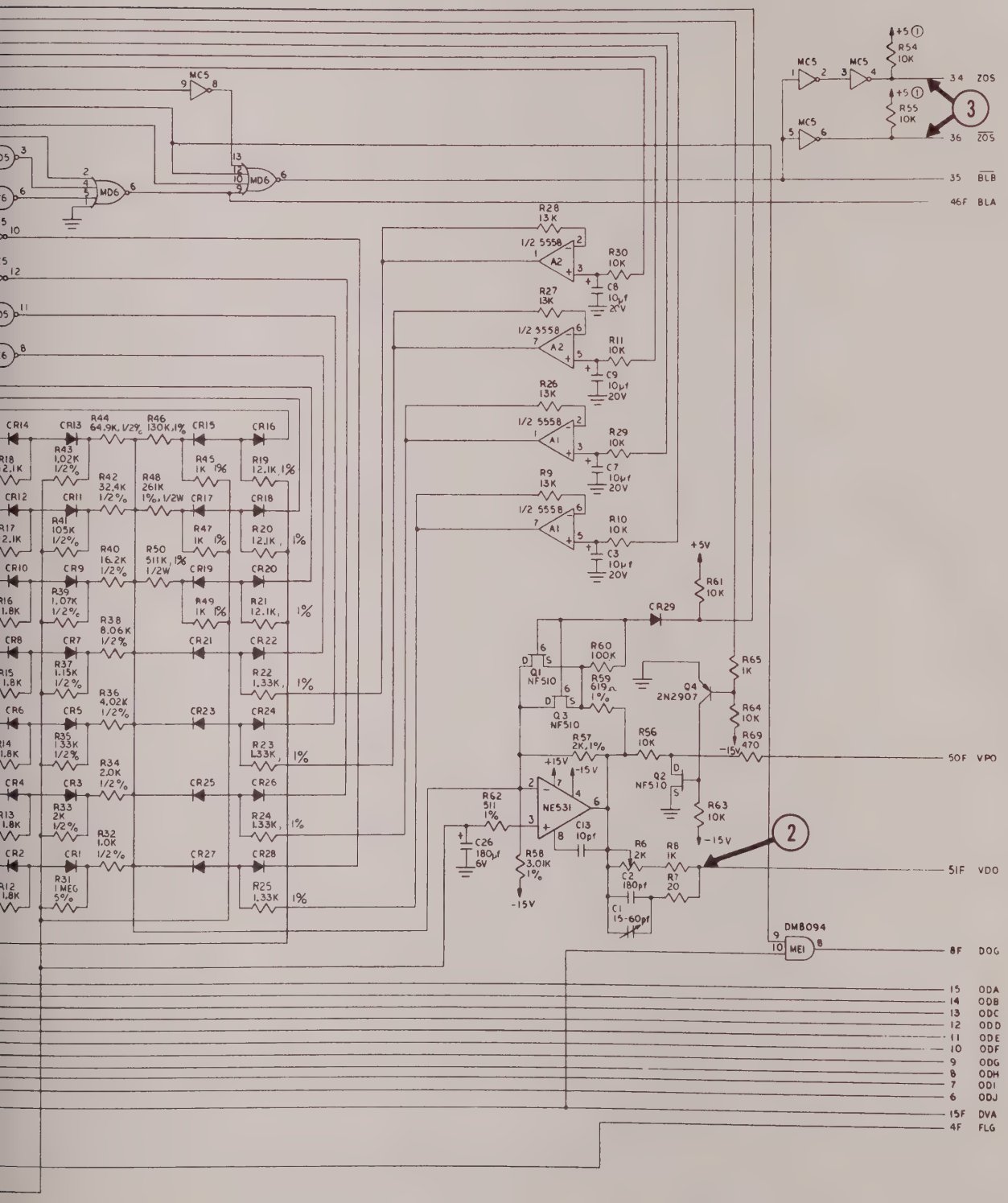
3. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. .5msec/div.
   Trigger: Int CH 1 — slope.
   1015: In display CH 1 & 3 on.
   CH 2 & 4 off. Display mode
   CH 1 - 4 vst.



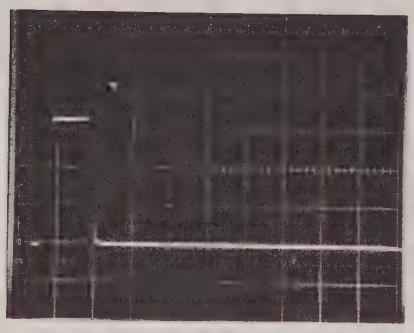

VXD 40
POL 41F
CVR 49F
CVF 48F
BVP 49
AVP 48
RIC 36F
DIO 45
ESR 46
XTD 47
XTB 41
XTA 36F
BCC 35F
AOC 42
BOO 42F
CCC 43
DOC 45F
XCL 43F
XCL 47F
XCK 44
XCK 44F
DSE 33
AMH 32
MOA 21
MOB 22
MOC 23
MOD 24
MOE 25
MOF 26
MOG 27
MOH 28
MOI 29
MOJ 30
ASA 31
XCB 34F
ADA 14F
APA 13F
ADB 12F
APB 10F
ADC 6F
APC 9F
+15V 16
-15V 39
+5V 4,5,50,51
ODP 11F
FLA 5F
DBV 40F
74174
74175
DM8094
C23 10µf 20V
C24 10µf 20V
C14-C16, C18, C20-C22 10µf 20V
R5 500
R4 500
R3 500
R2 500
R1 500
C6 0.1
1



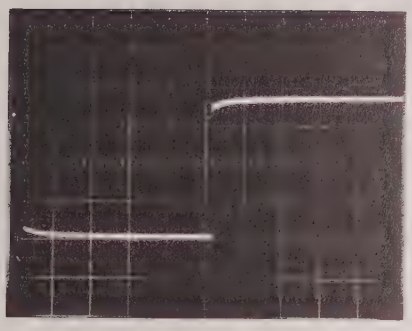




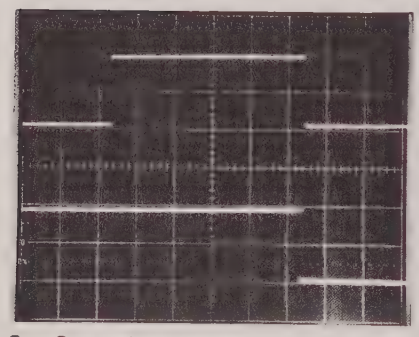
Y Output D/A & I/O



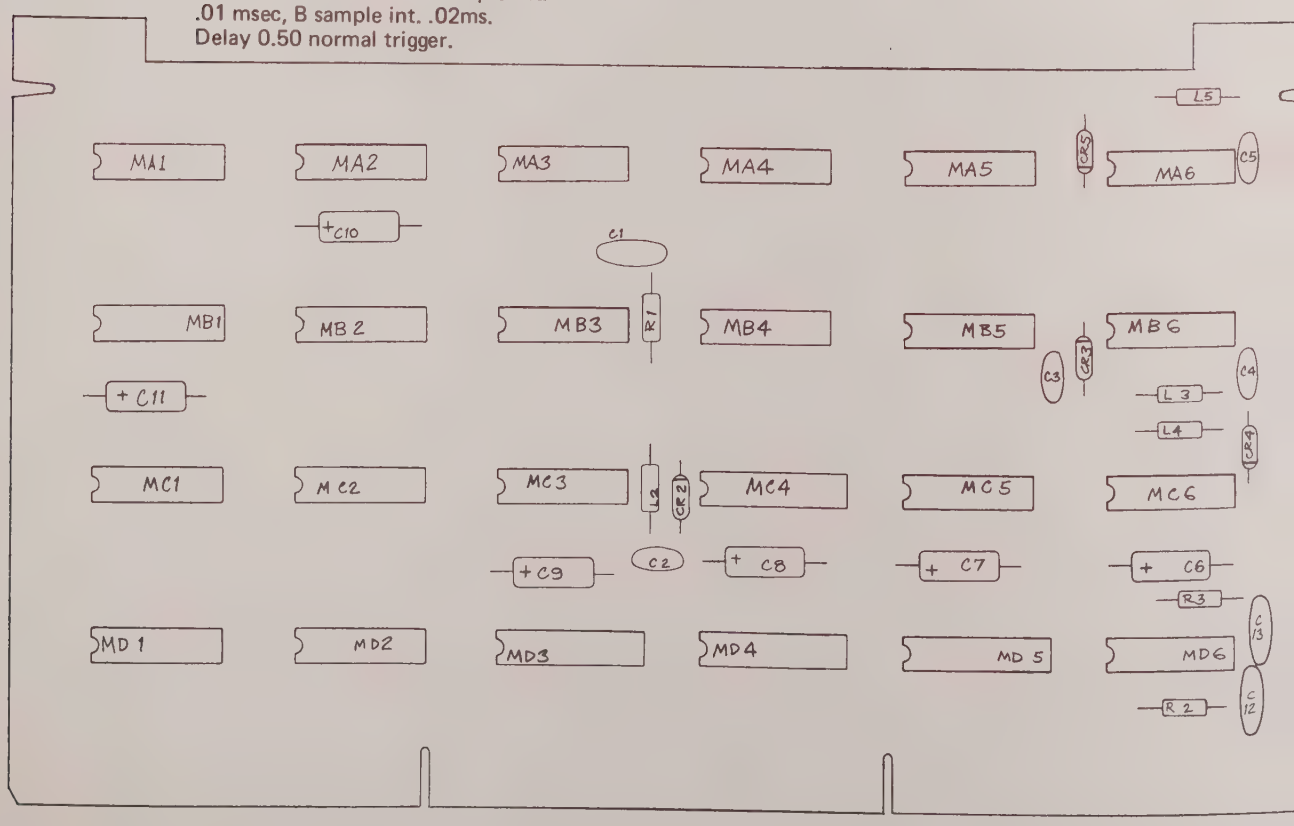
1. Scope: Vert. 1 v/div, Horz. .1μsec/div.
   Trigger: Int + slope.
   1015: Trig mode normal. 1kHz wave input.

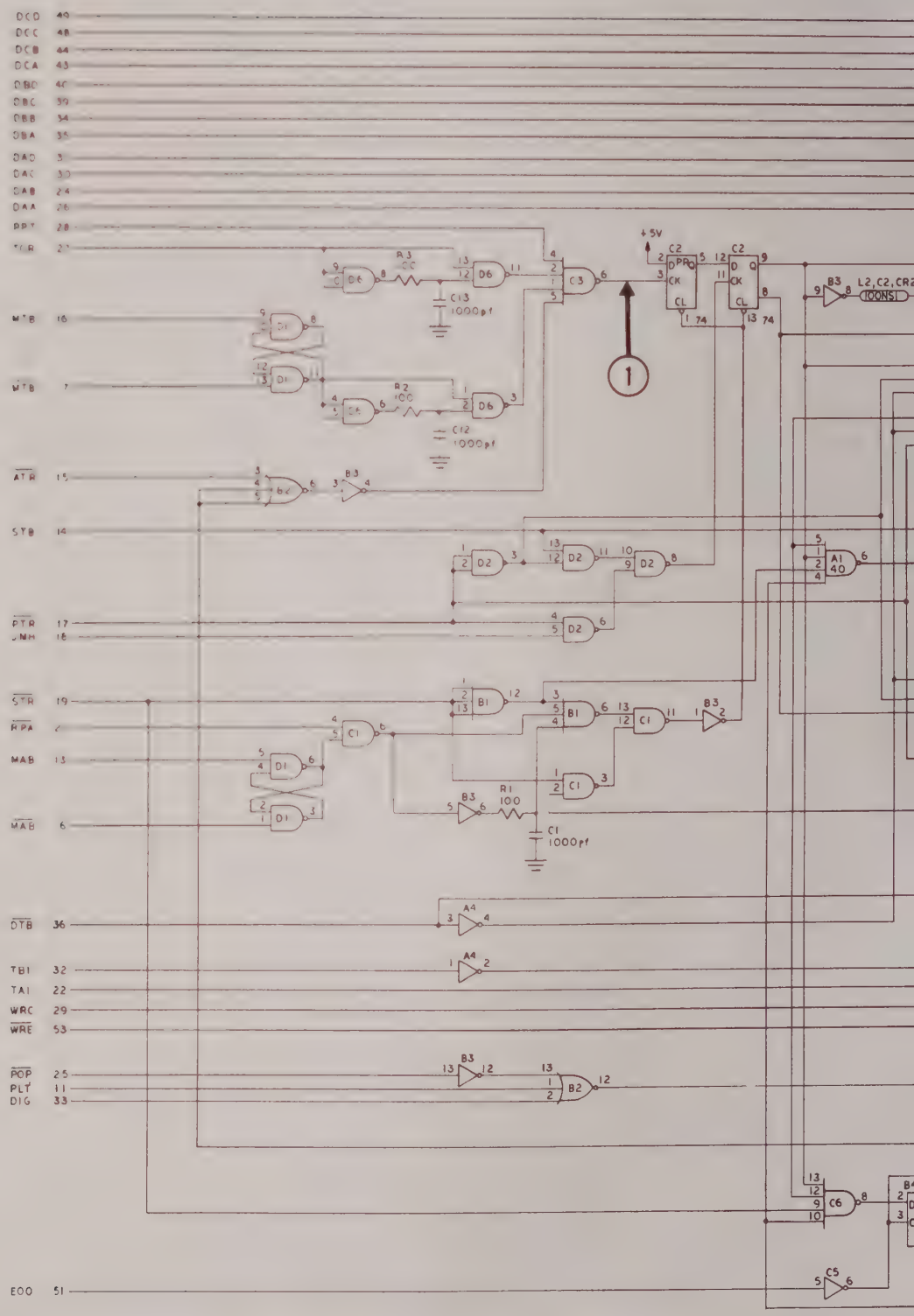


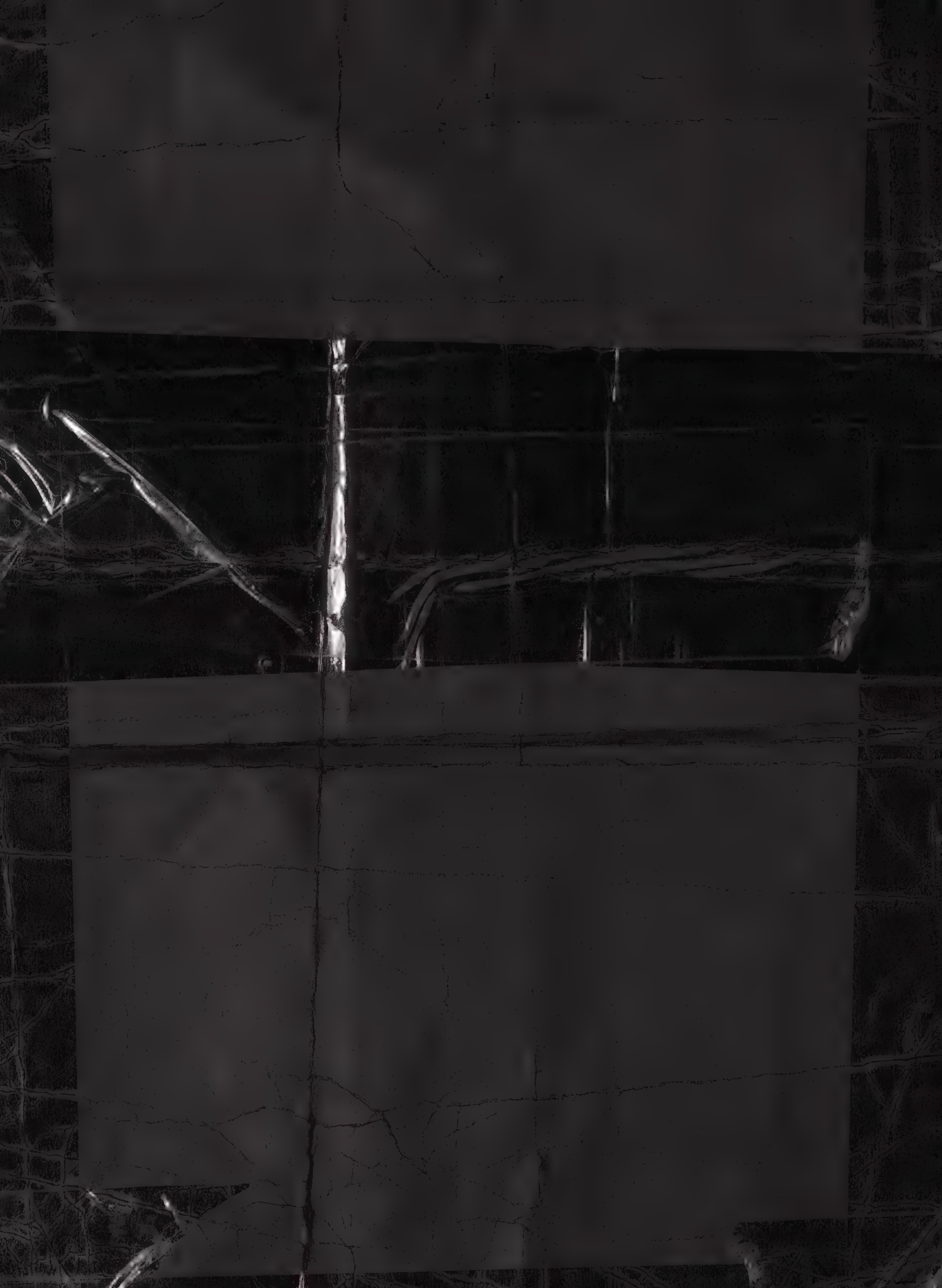
2. Scope: Vert. 1 v/div, Horz. 20 μsec/div.
   Trigger: Int – slope.
   1015: Auto trigger delay 0.00.

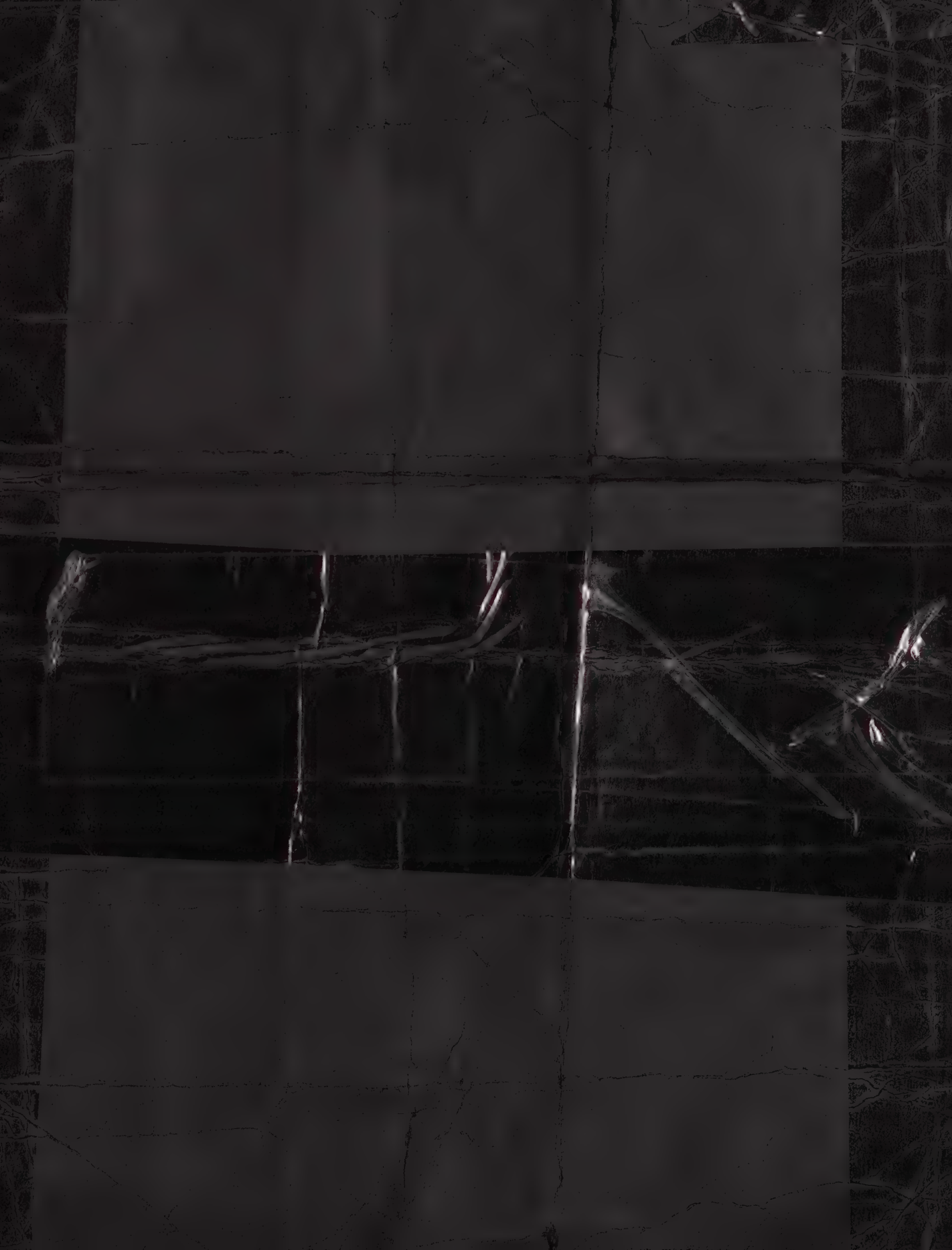


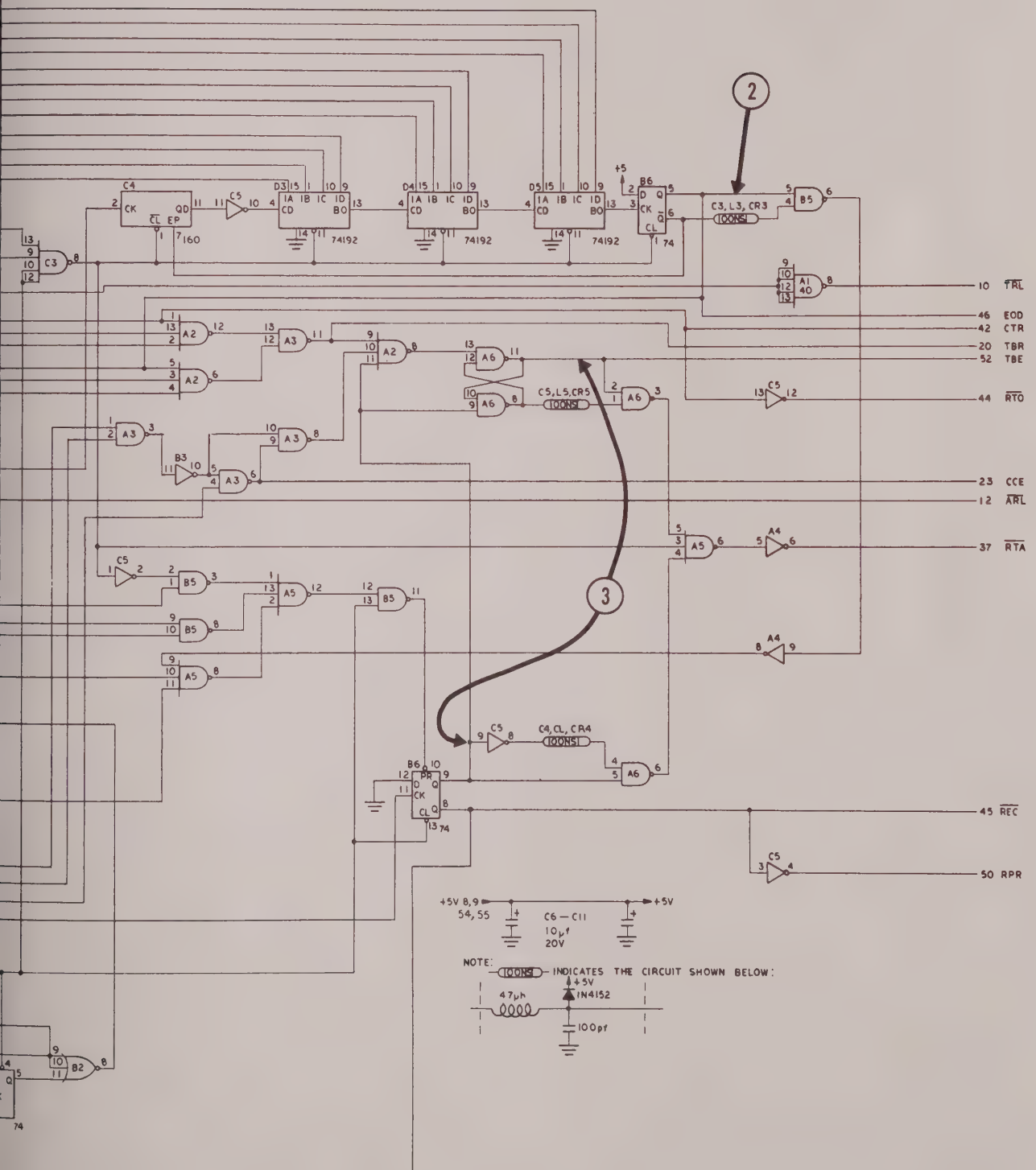
3. Scope: Vert. CH 1 & 2 2 v/div, Horz. 2msec/div.
   Trigger: Int CH 2 (B6 Pin 9)
   1015: Dual TB mode. A sample Int. .01 msec, B sample int. .02ms. Delay 0.50 normal trigger.

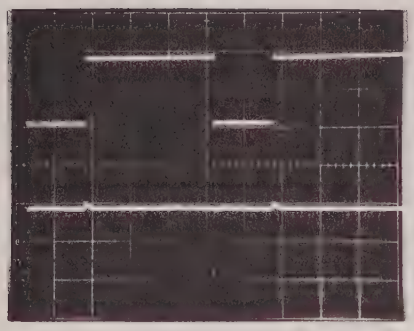



DCD 40
DCC 48
DCB 44
DCA 43
DBD 40
DBC 39
DBB 34
DBA 35
DAD 3
DAC 33
DAB 24
DAA 26
PPT 28
TCR 27
MTB 16
MTB 7
ATR 15
STB 14
PTR 17
JNM 18
STR 19
RPA 2
MAB 13
MAB 6
DTB 36
TBI 32
TAI 22
WRC 29
WRE 53
POP 25
PLT 11
DIG 33
EOO 51
+5V
R3 CC
C13 1000pf
R2 100
C12 1000pf
R1 100
C1 1000pf
L2,C2,CR2
TOONS1
1
74
74

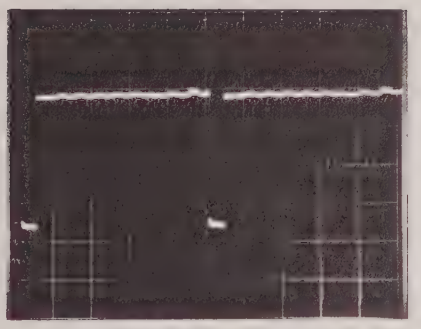




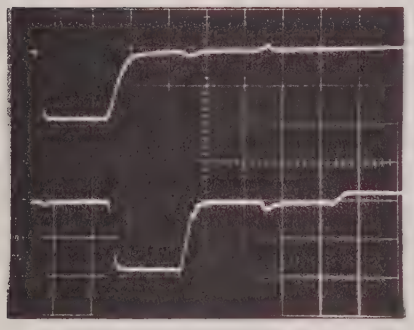

2
3
C4
7160
74192
74192
74192
C3, L3, CR3
100NS
C5, L5, CR5
100NS
C4, L4, CR4
100NS
10 TRL
46 EOD
42 CTR
20 TBR
52 TBE
44 RTO
23 CCE
12 ARL
37 RTA
45 REC
50 RPR
+5V 8,9
54, 55
C6 — C11
10μf
20V
+5V
NOTE:
100NS INDICATES THE CIRCUIT SHOWN BELOW:
+5V
47μh
IN4152
100pf



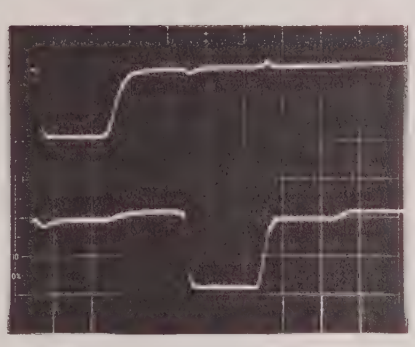
1. Scope: Vert. CH 1 & 2 2 v/div, Horz. 2μsec/div.
Trigger: Int CH 2
1015: Pretrig Record Mode, sample Interval .01msec, unit armed.



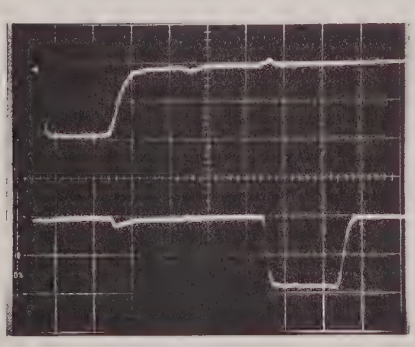
2. Scope: Vert. 1 v/div, Horz. 2μsec/div.
Trigger: Int – slope.
1015: Pretrig Record, sample interval .01msec, unit armed.



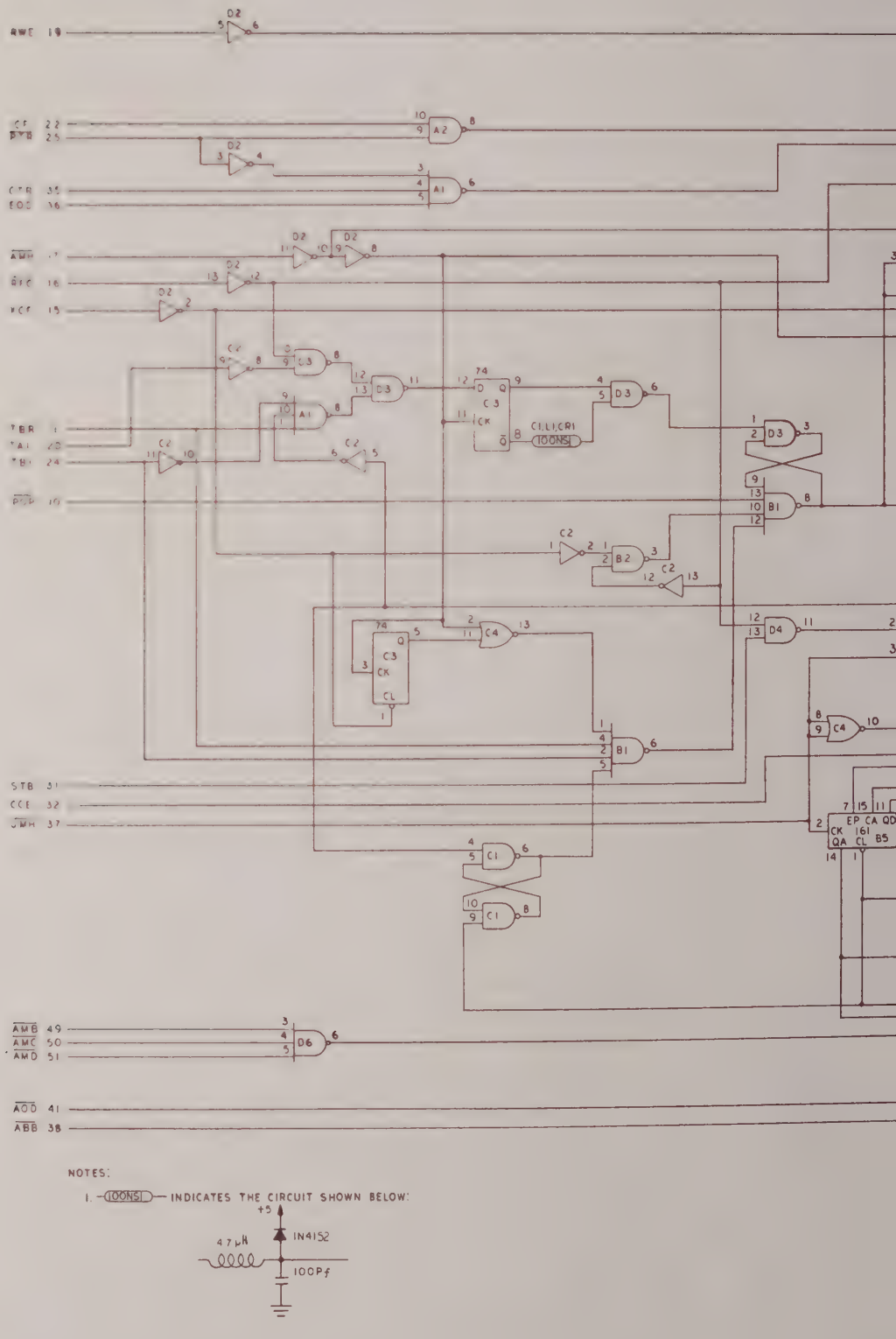
3. Scope: Vert. CH 1 & 2 2 v/div, Horz. .1μsec/div.
Trigger: Int CH 1 – slope.
1015: Pretrig Record, sample interval .01msec, unit armed.



4. Scope: Vert. CH 1 & 2 2 v/div, Horz. .1μsec/div.
Trigger: Int CH 1 – slope.
1015: Pretrig Record, sample interval .01msec, unit armed.

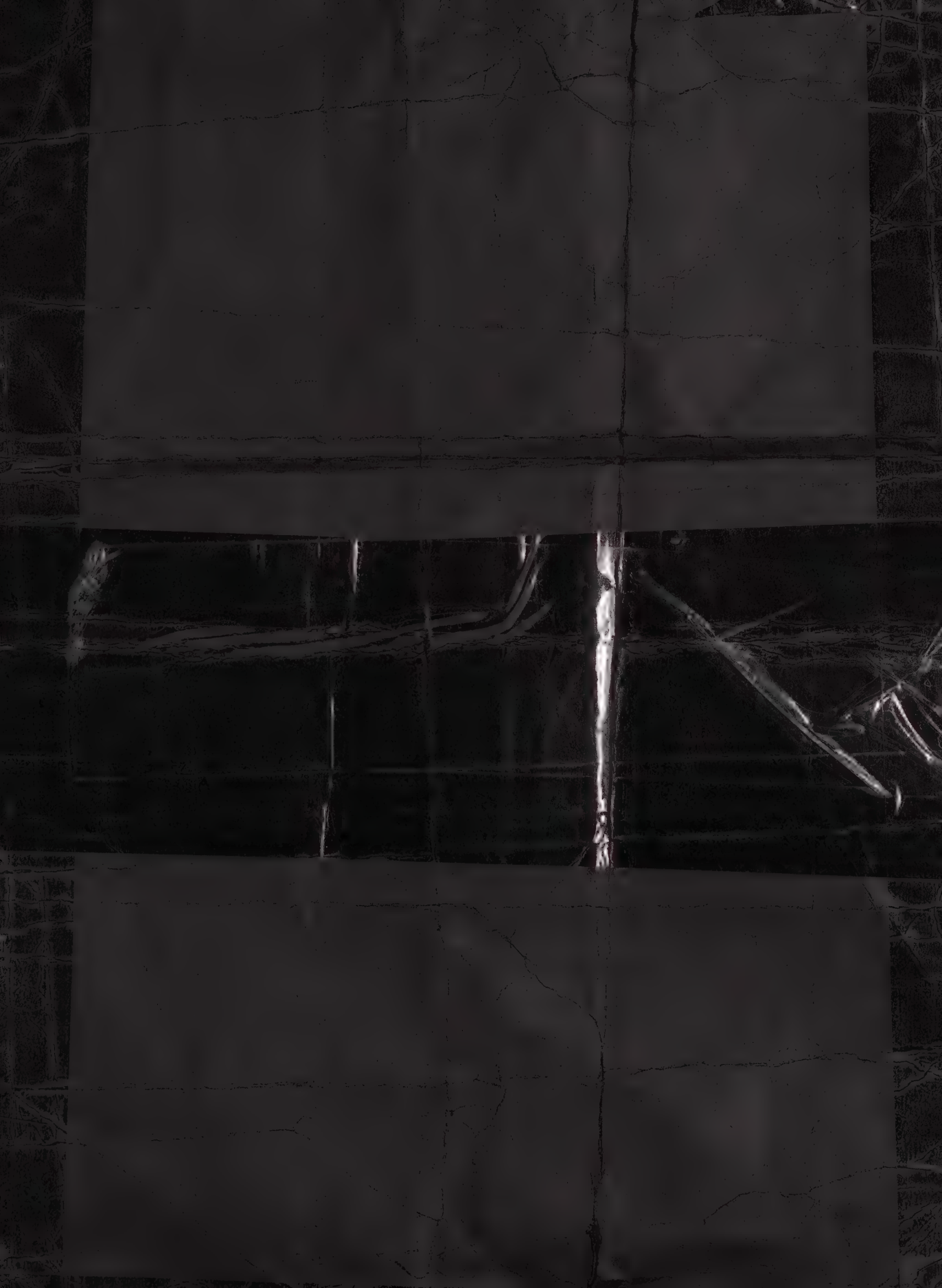


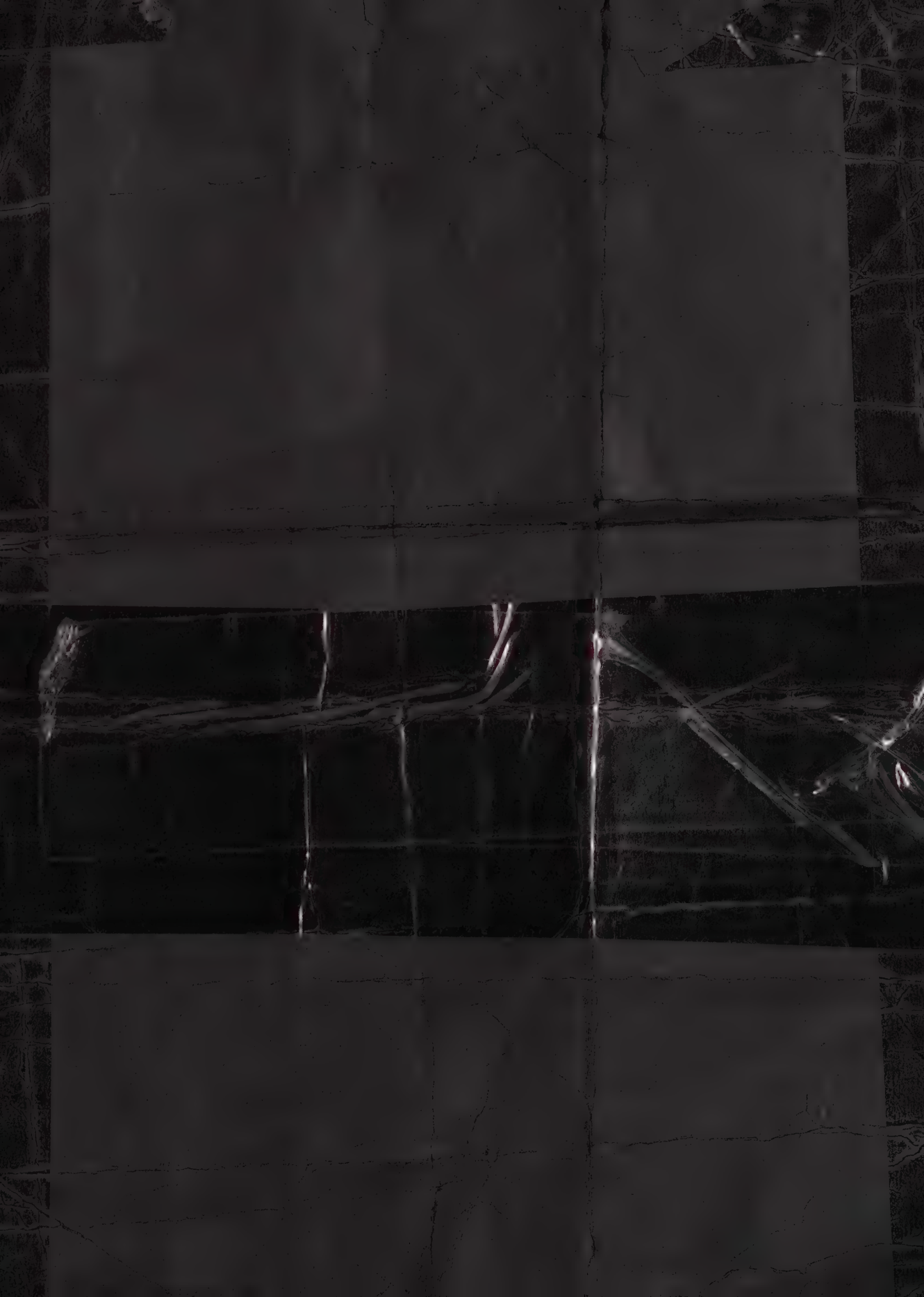
5. Scope: Vert. CH 1 & 2 2 v/div, Horz. .1μsec/div.
Trigger: Int CH 1 – slope.
1015: Pretrig Record, sample interval .01msec, unit armed.

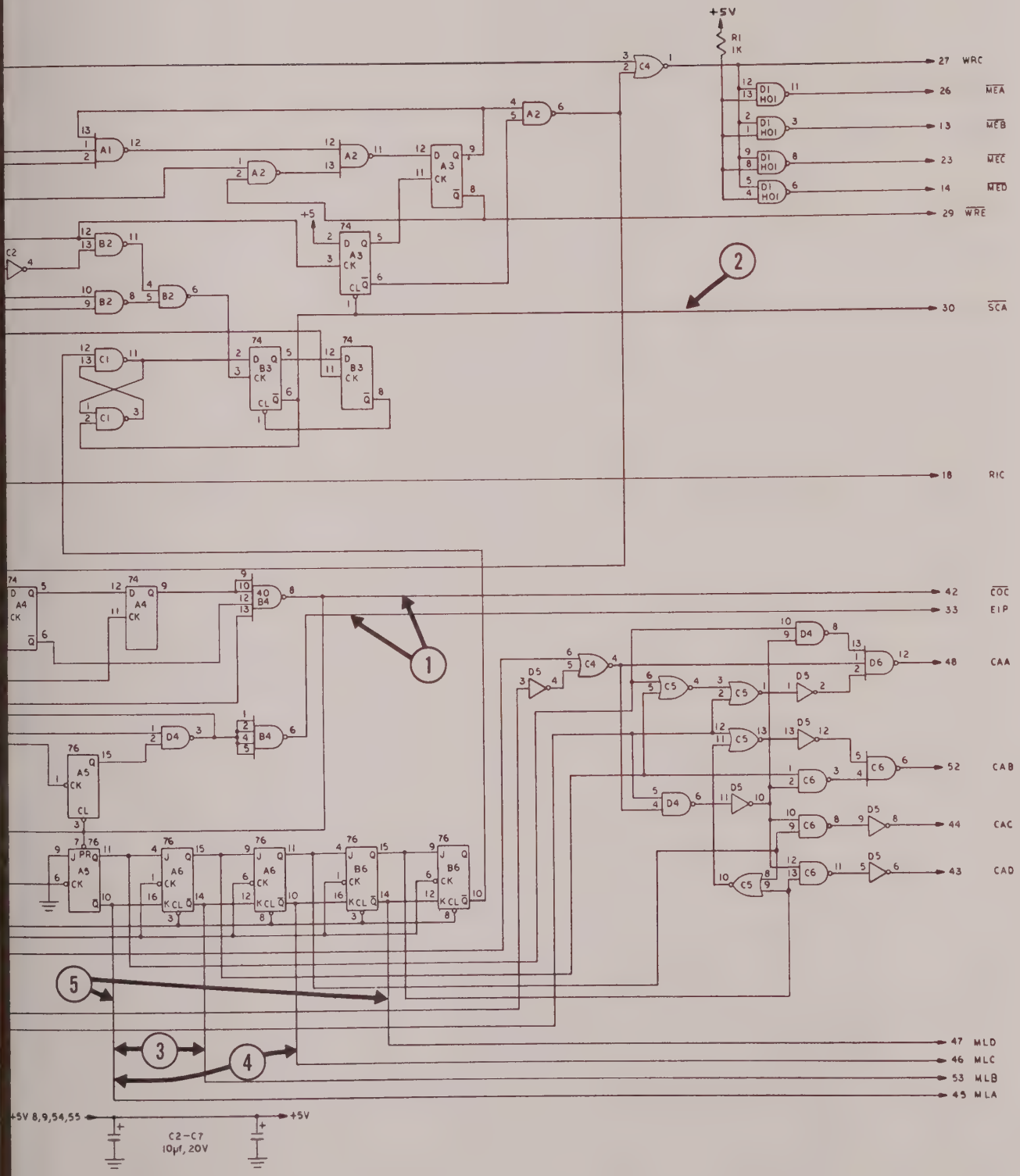


NOTES:

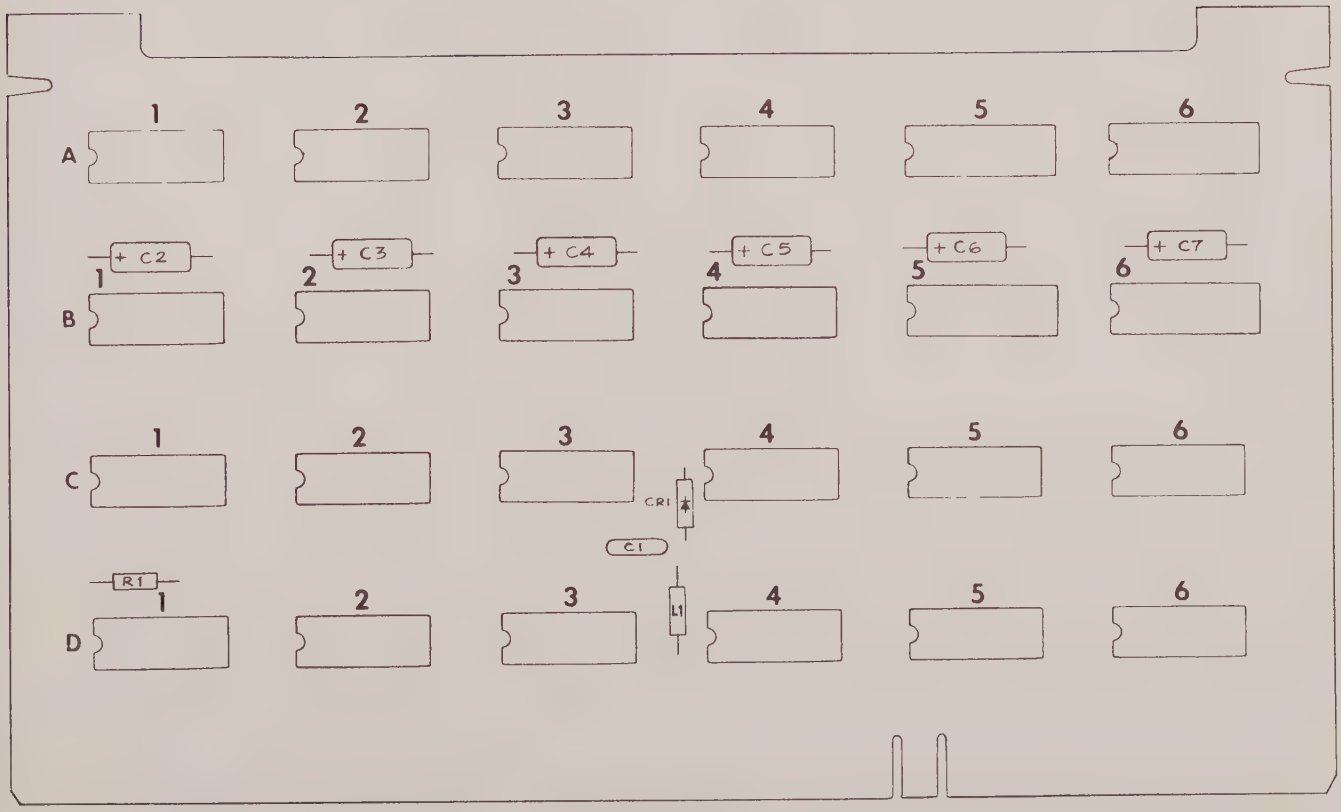
1. (100NS) — INDICATES THE CIRCUIT SHOWN BELOW:



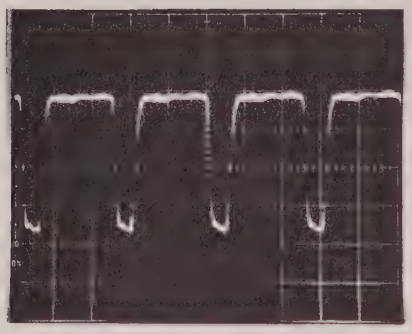




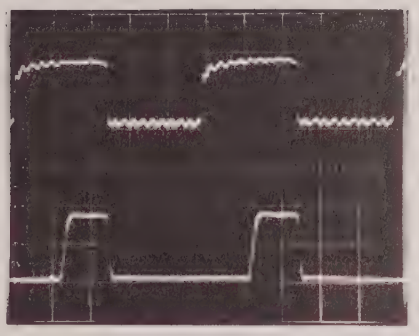
Record Control
-100-



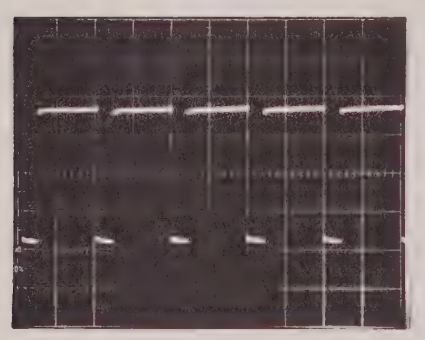
Record Control
-100A-



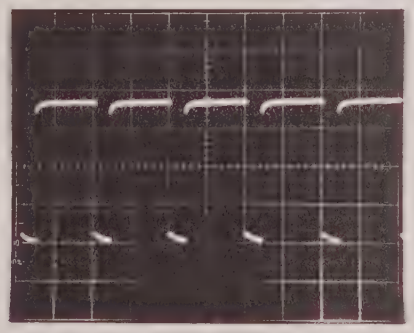
1. Scope: Vert. 1 v/div, Horz. .1μsec/div.
Trigger: Int – slope.



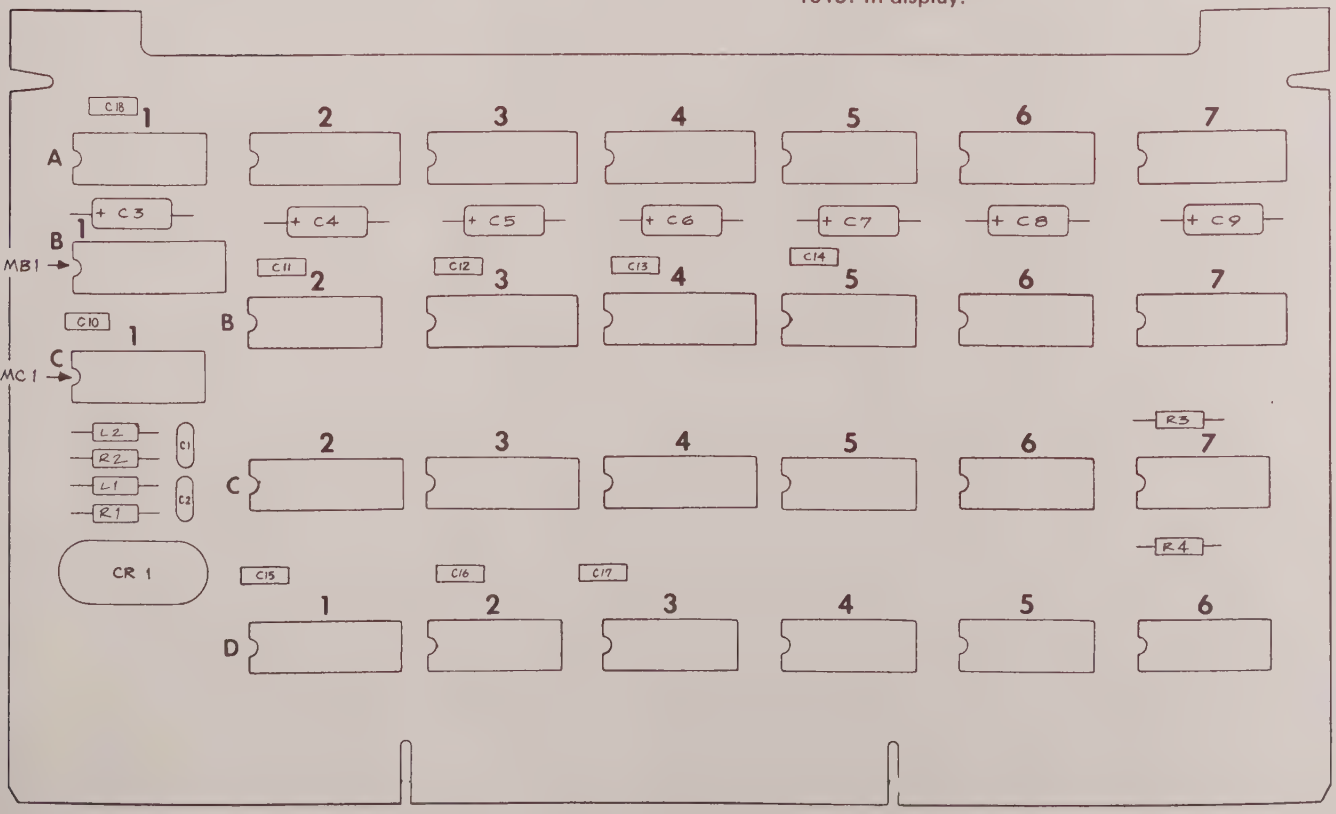
2. Scope: Vert. CH 1 & 2 2 v/div,
Horz. .2μsec/div.
Trigger: Int CH 1 + scope.
1015:

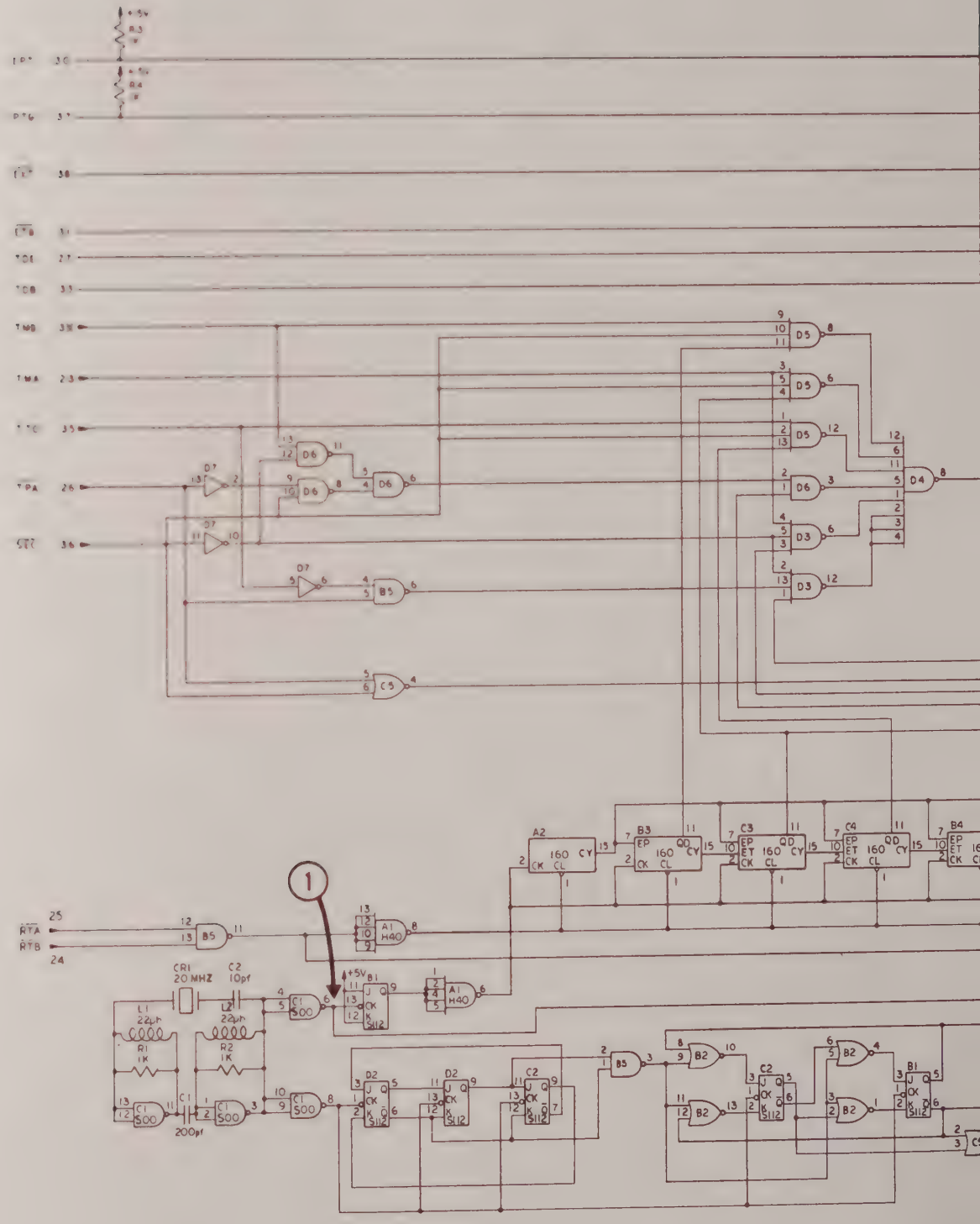


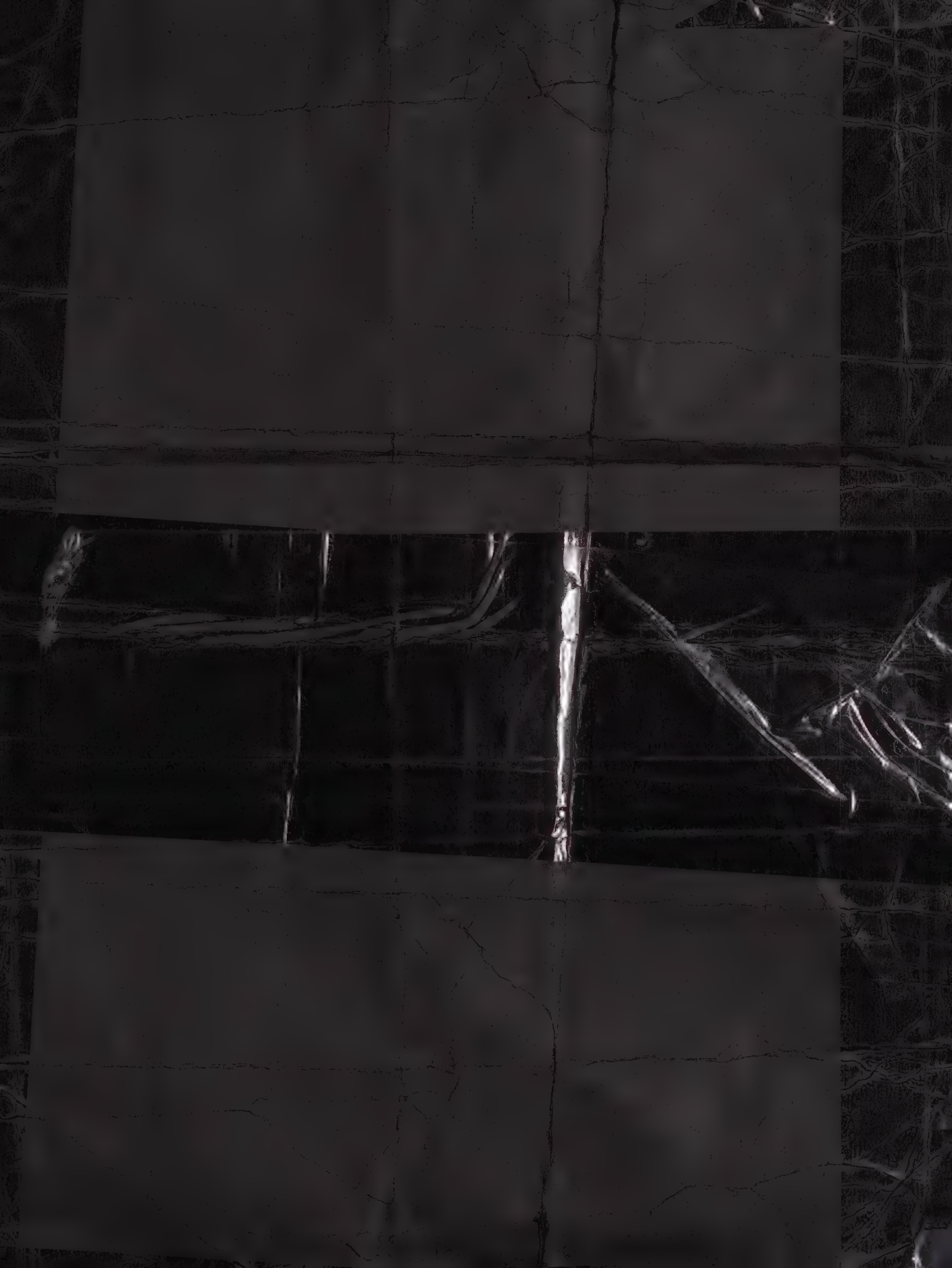
3. Scope: Vert. 1 v/div, Horz. 5μsec/div.
Trigger: Int – slope.
1015: Sample Interval .01 msec.

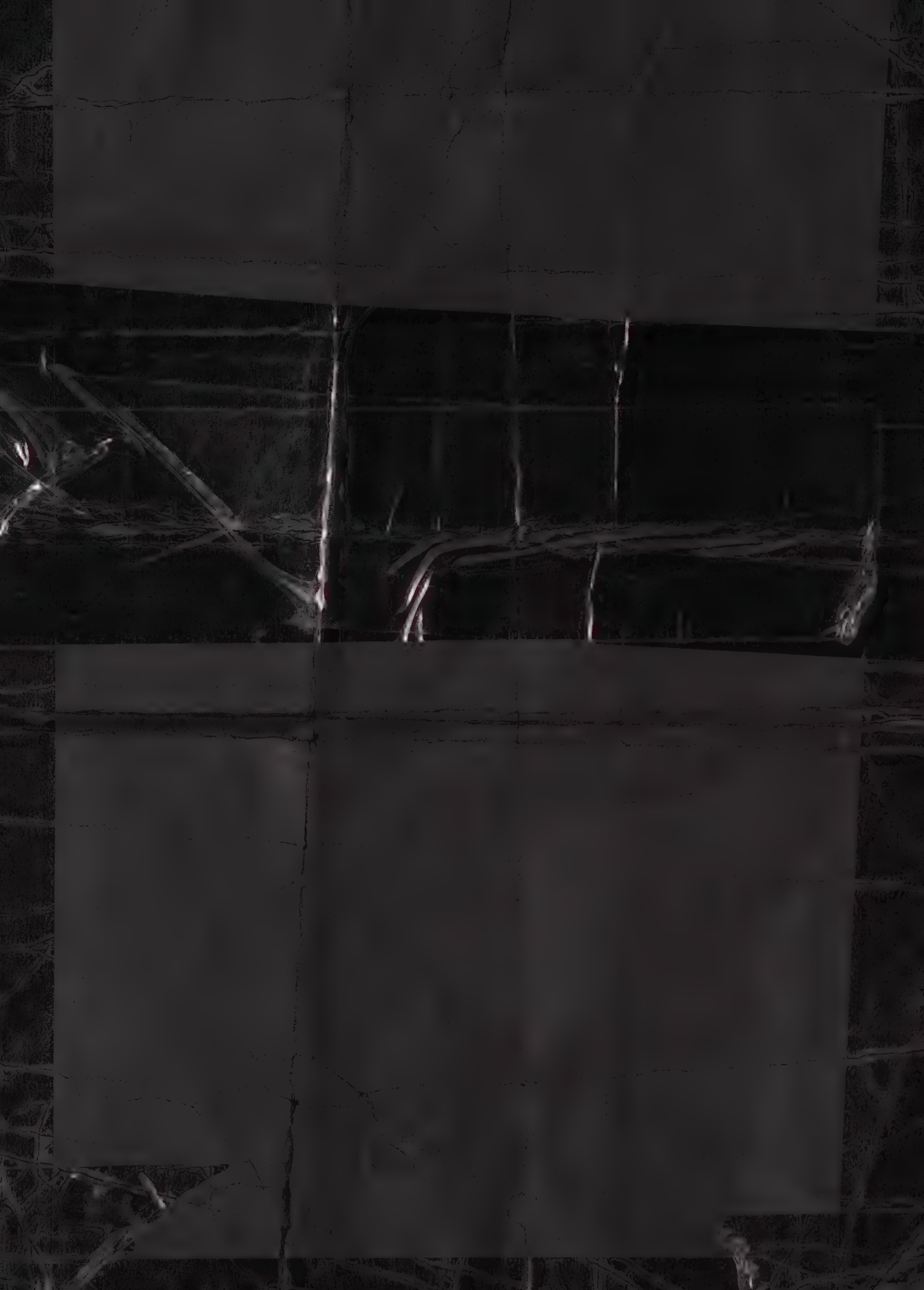


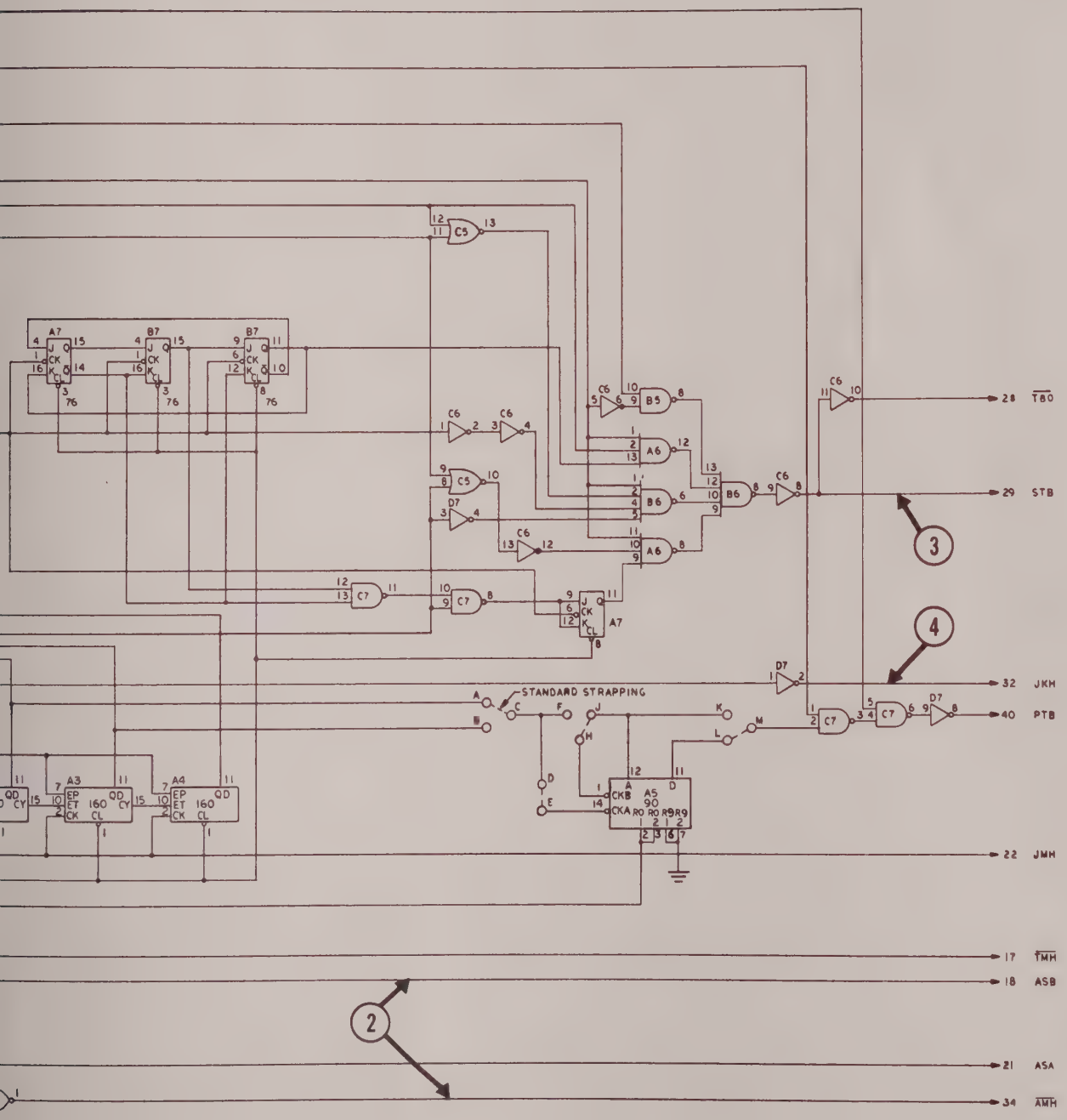
4. Scope: Vert. 1 v/div, Horz. 50
μsec/div.
Trigger: Int – slope.
1015: In display.

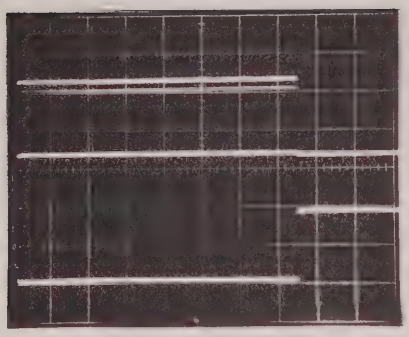



1
CR1
20 MHZ
C2
10pf
L1
22μh
L2
22μh
R1
1K
R2
1K
200pf
+5V
RTA
RTB
25
24
A2
B3
C3
C4
160 CY
CK CL
EP ET
QD CY

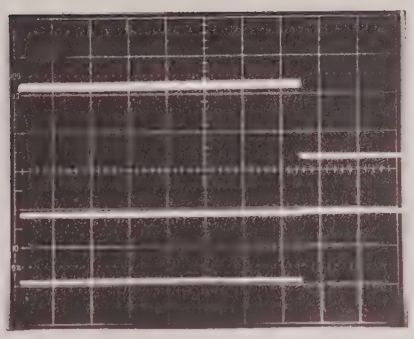




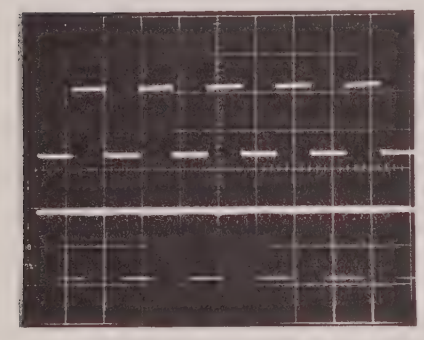

STANDARD STRAPPING
28 TBO
29 STB
32 JKH
40 PTB
22 JMH
17 TMH
18 ASB
21 ASA
34 AMH
2
3
4



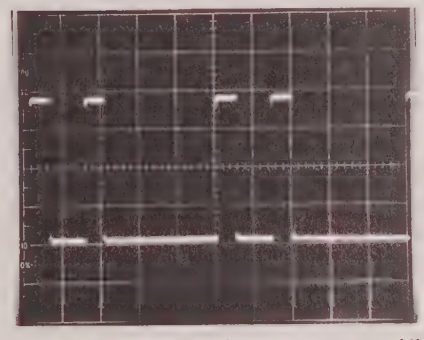
1. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. 1msec/div.
   Trigger: Int. CH 2 – slope.
   1015: Auto digital. 2μsec CMD rate
   Trigger mode normal. Sample interval
   .01msec.



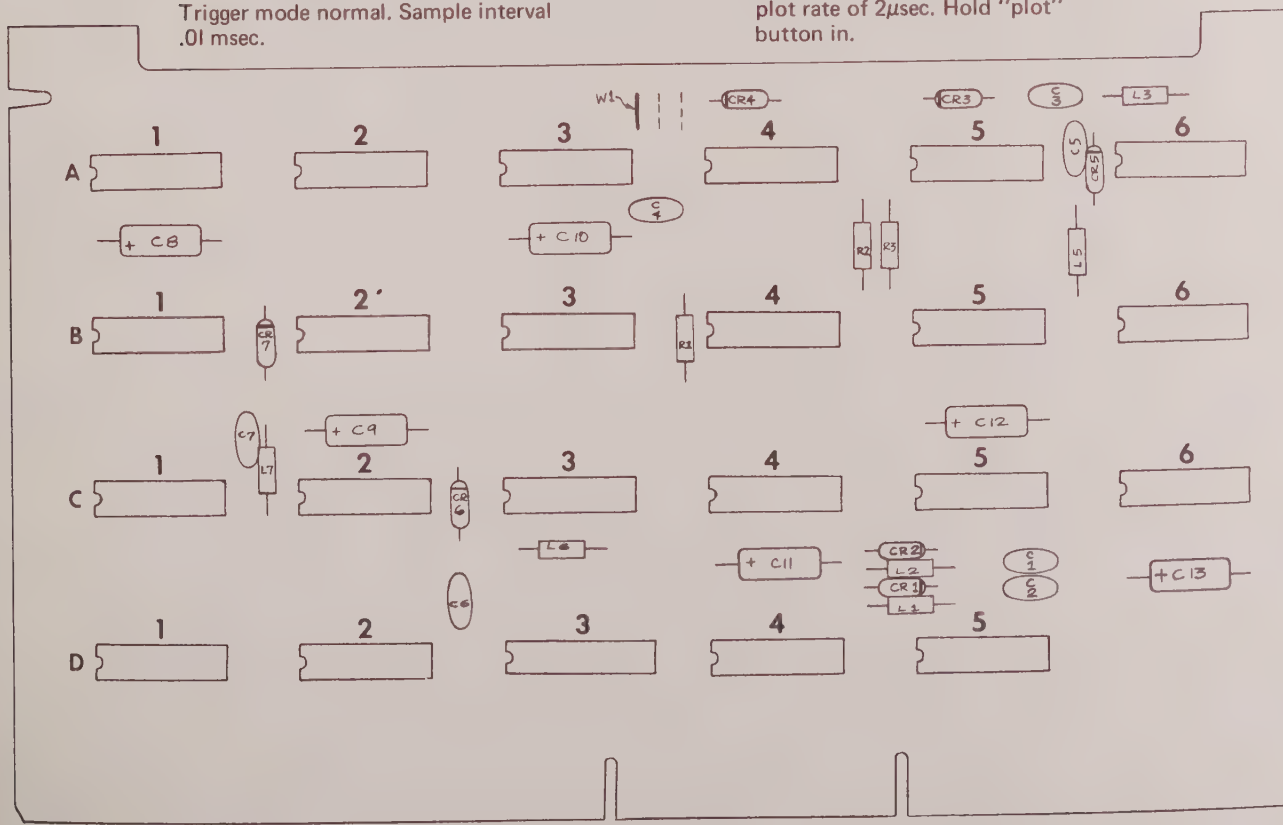
2. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. 1msec/div.
   Trigger: Int. CH 2 – slope.
   1015: Auto digital. 2μsec CMD rate.
   Trigger mode normal. Sample interval
   .01 msec.

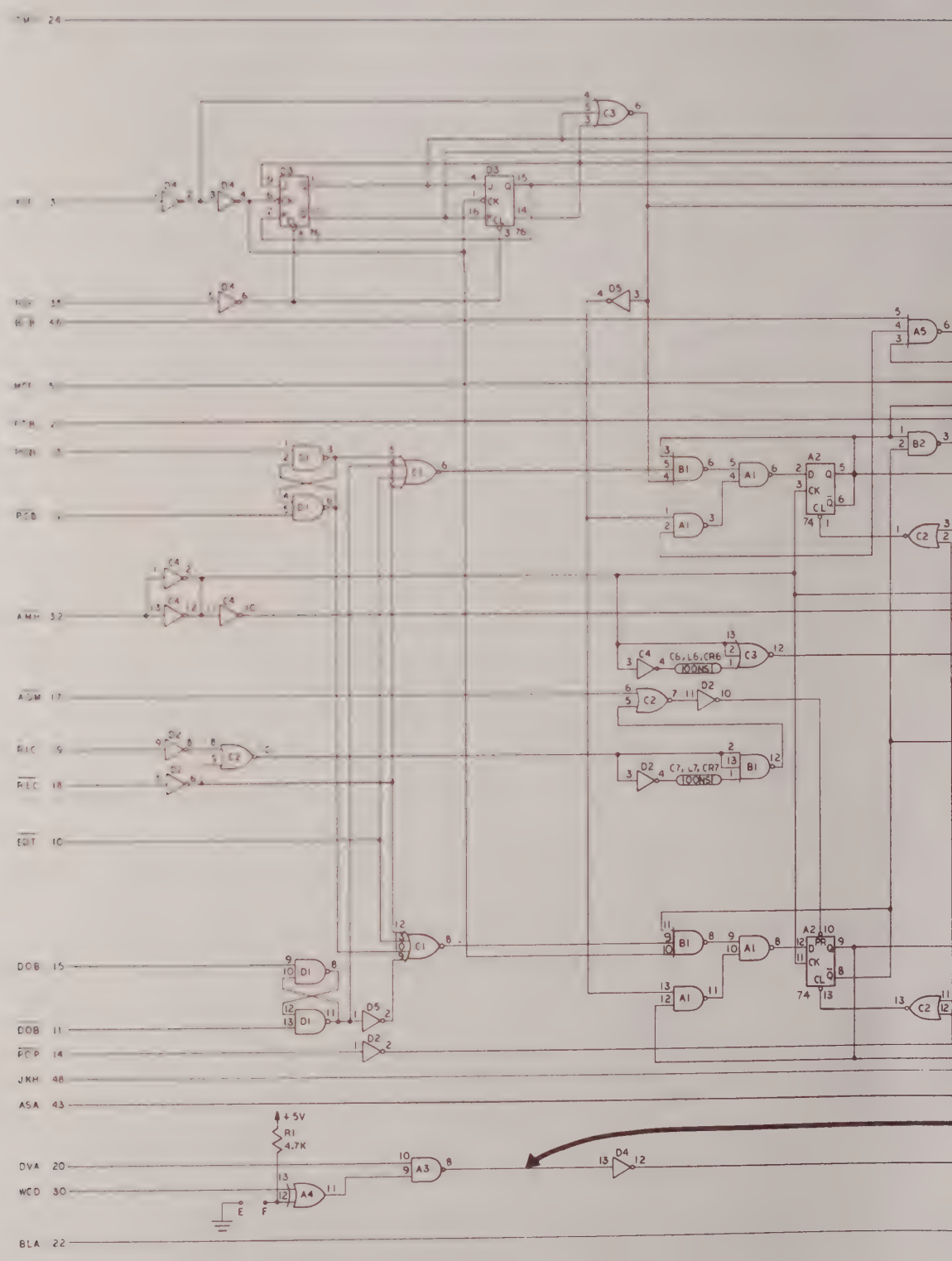


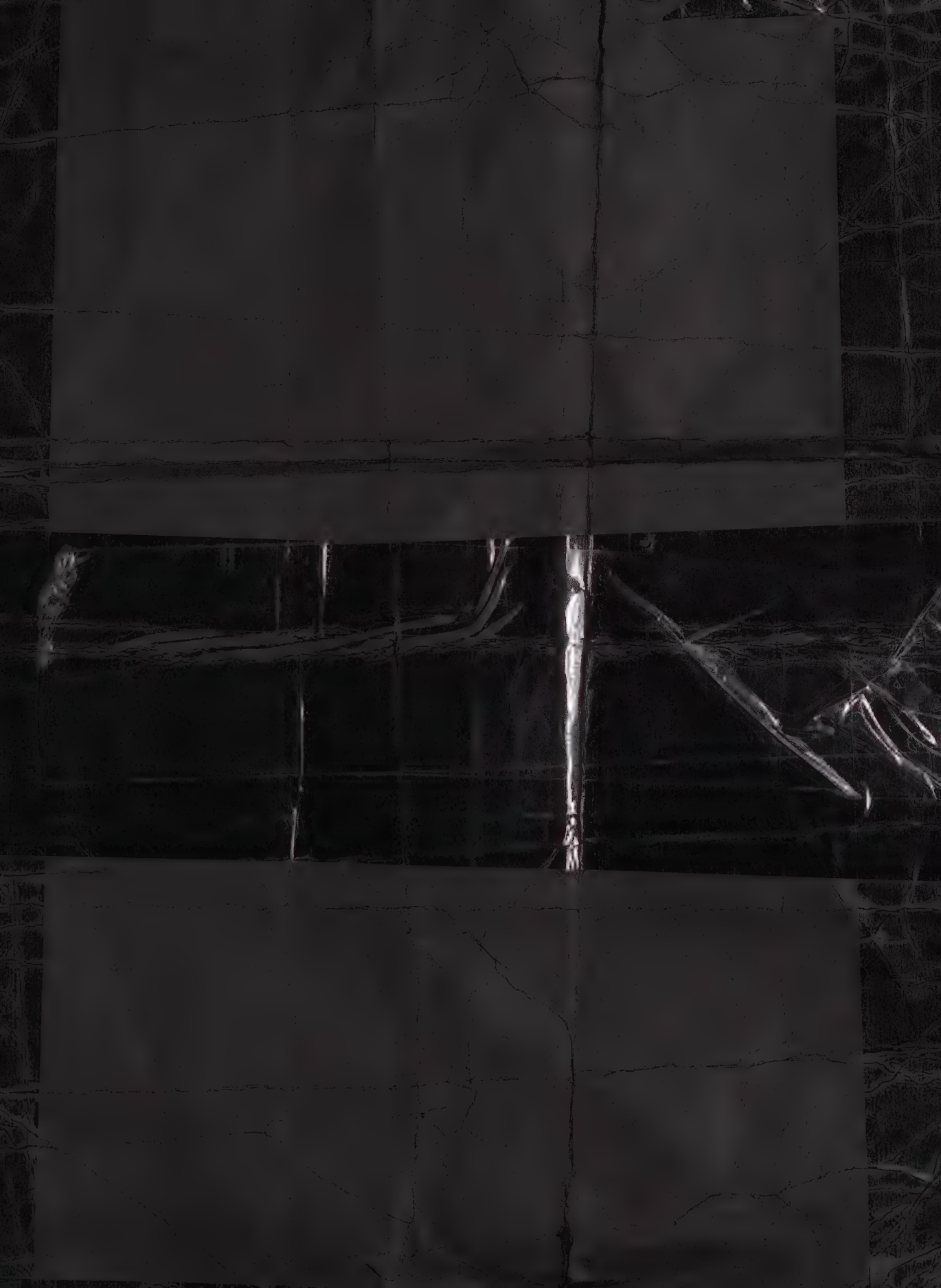
3. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. 1μsec/div.
   Trigger: Int. CH 1 – slope.
   1015: Auto digital. 2μsec CMD rate.
   Trigger mode normal. Sample interval
   .01 msec.

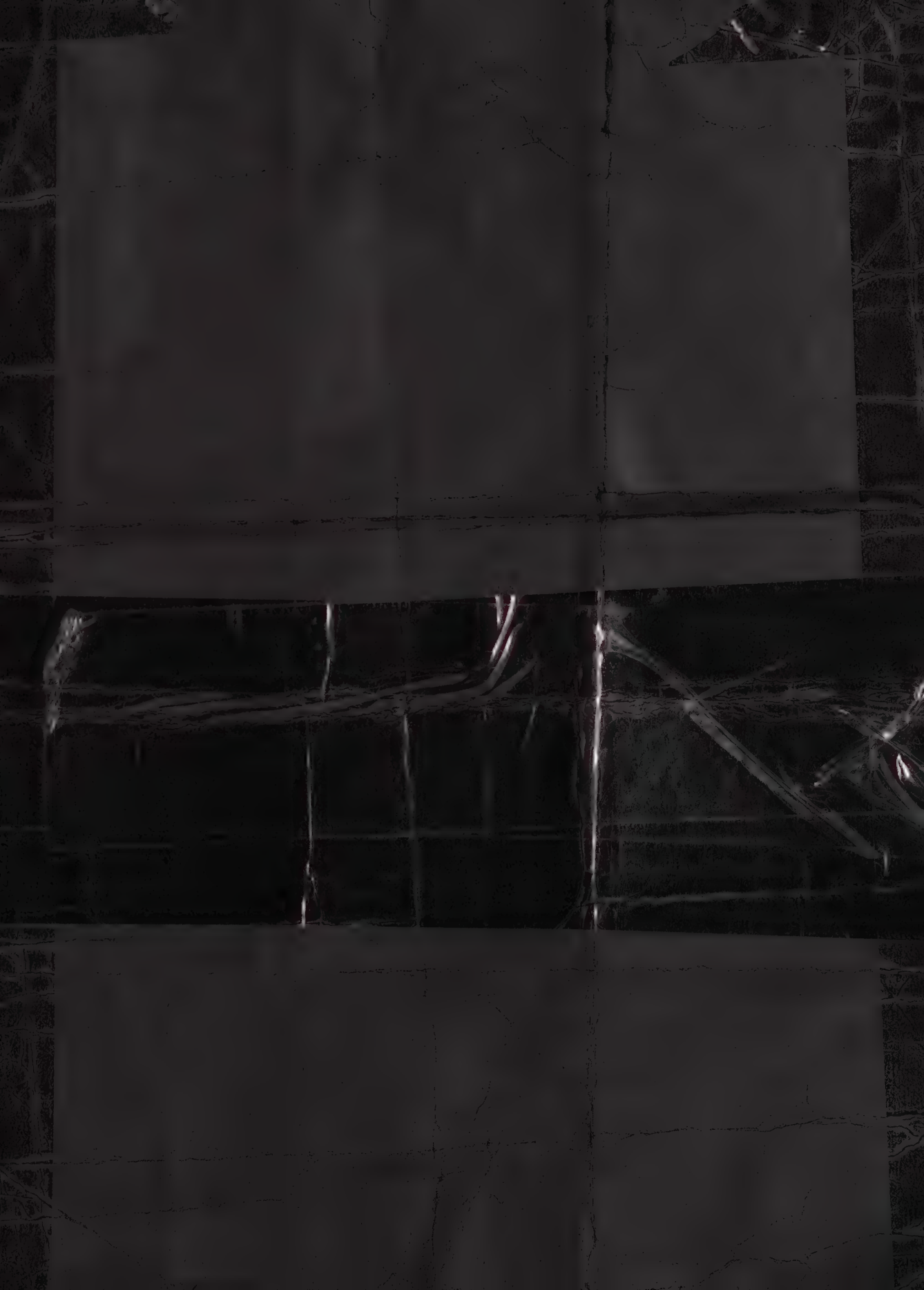


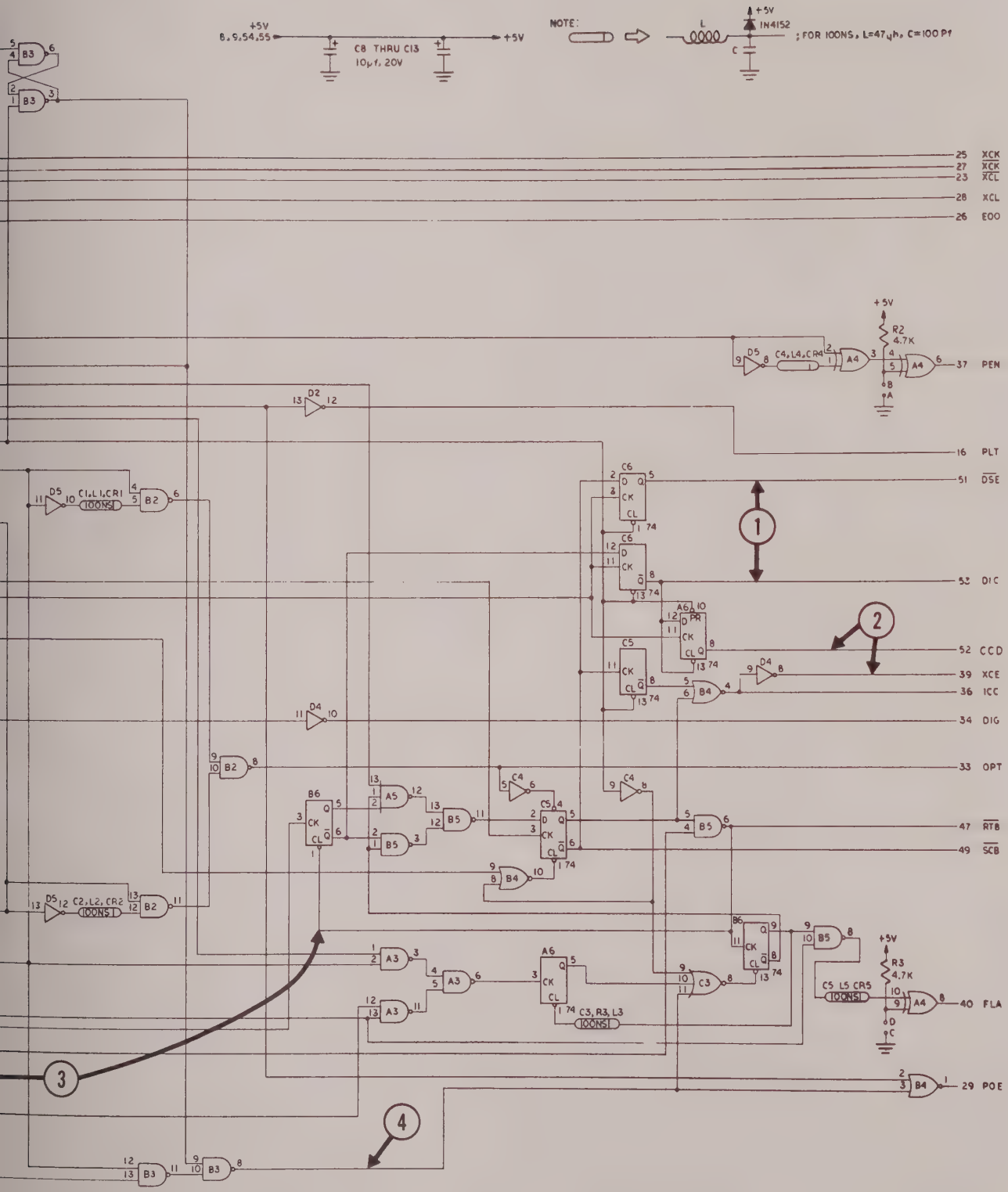
4. Scope: Vert. 1 v/div, Horz. 2msec/div.
   Trigger: Int + slope.
   1015: Edit mode, CH 1 – 4 vst,
   Chan. 1 & 3 on, CH 2 & 4 off. Ext
   plot rate of 2μsec. Hold "plot"
   button in.



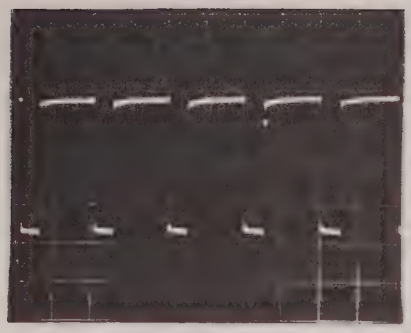

DOB 15
DOB 11
BCP 14
JKH 48
ASA 43
DVA 20
WCD 30
BLA 22
+5V
R1
4.7K
C6, L6, CR6
C7, L7, CR7
TOGGLE



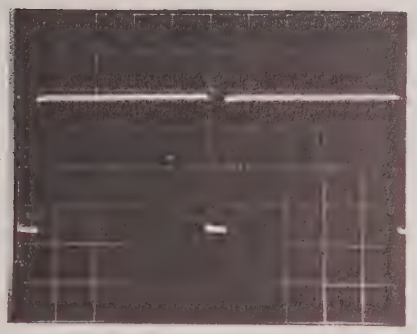




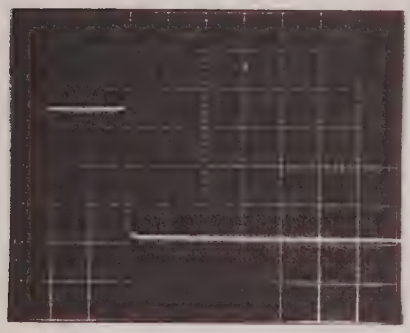
Output Control



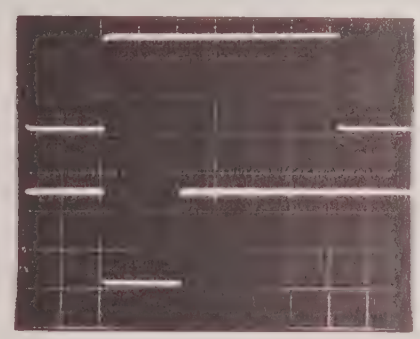
1. Scope: Vert. 1 v/div, Horz. .5 sec/div
   Trigger: Int – slope
   1015: In display mode.



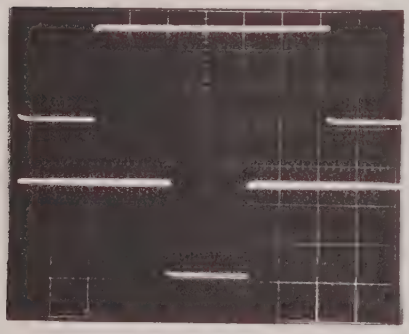
2. Scope: Vert. 1 v/div, Horz. 2μsec/div
   Trigger: Int – slope
   1015: Pretrig record mode sample interval .01msec. Unit armed.



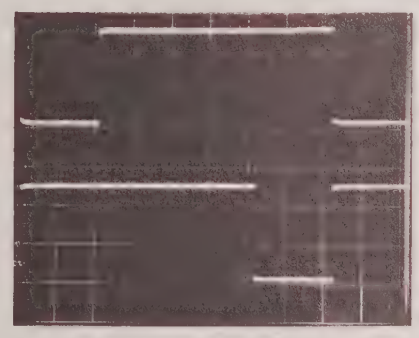
3. Scope: Vert. 1 v/div, Horz .1μsec/div
   Trigger: Int + slope
   1015: In display mode.



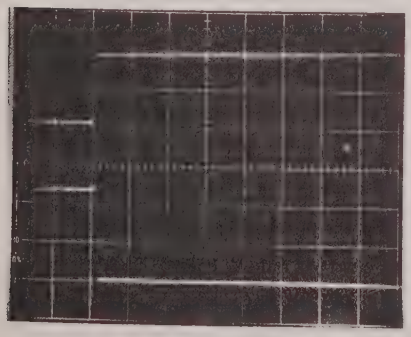
4. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. .5msec/div
   Trigger: Int CH 1
   Display mode CH 1 – 4 vst



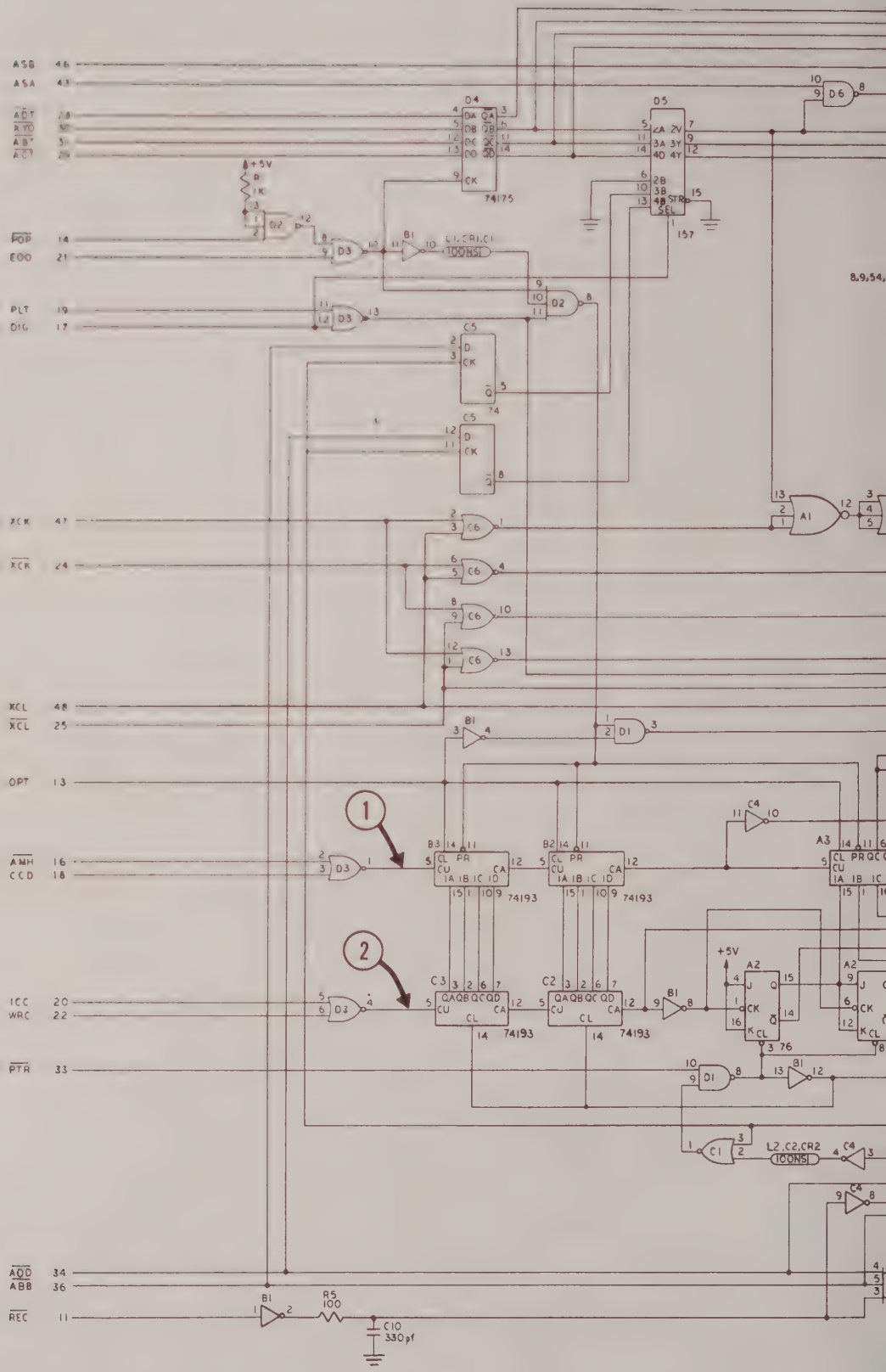
5. Scope: Vert, CH 1 & 2 2 v/div,
   Horz. .5msec/div
   Trigger: Int CH 1
   1015: Display mode CH 1 - 4 vst

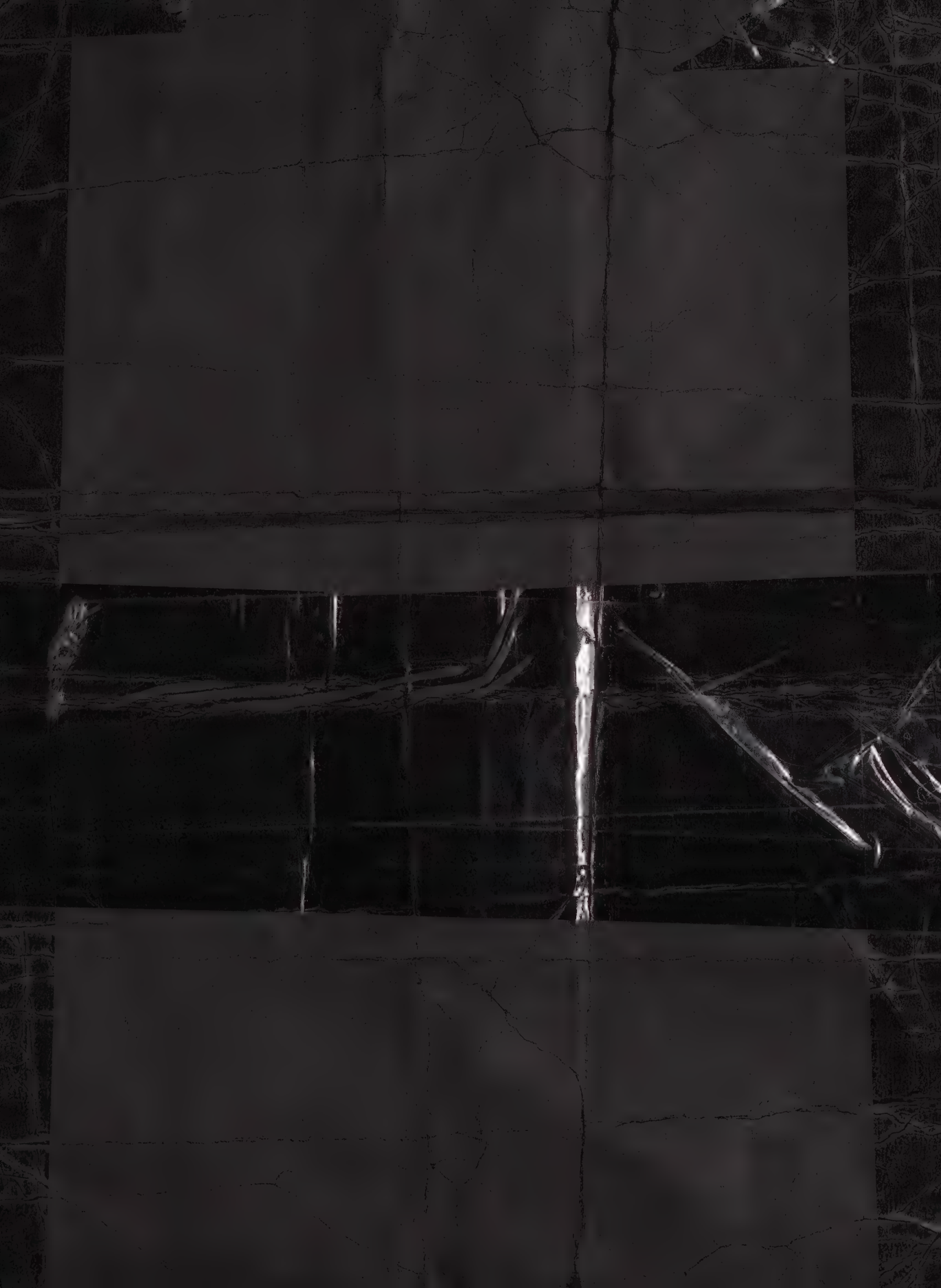


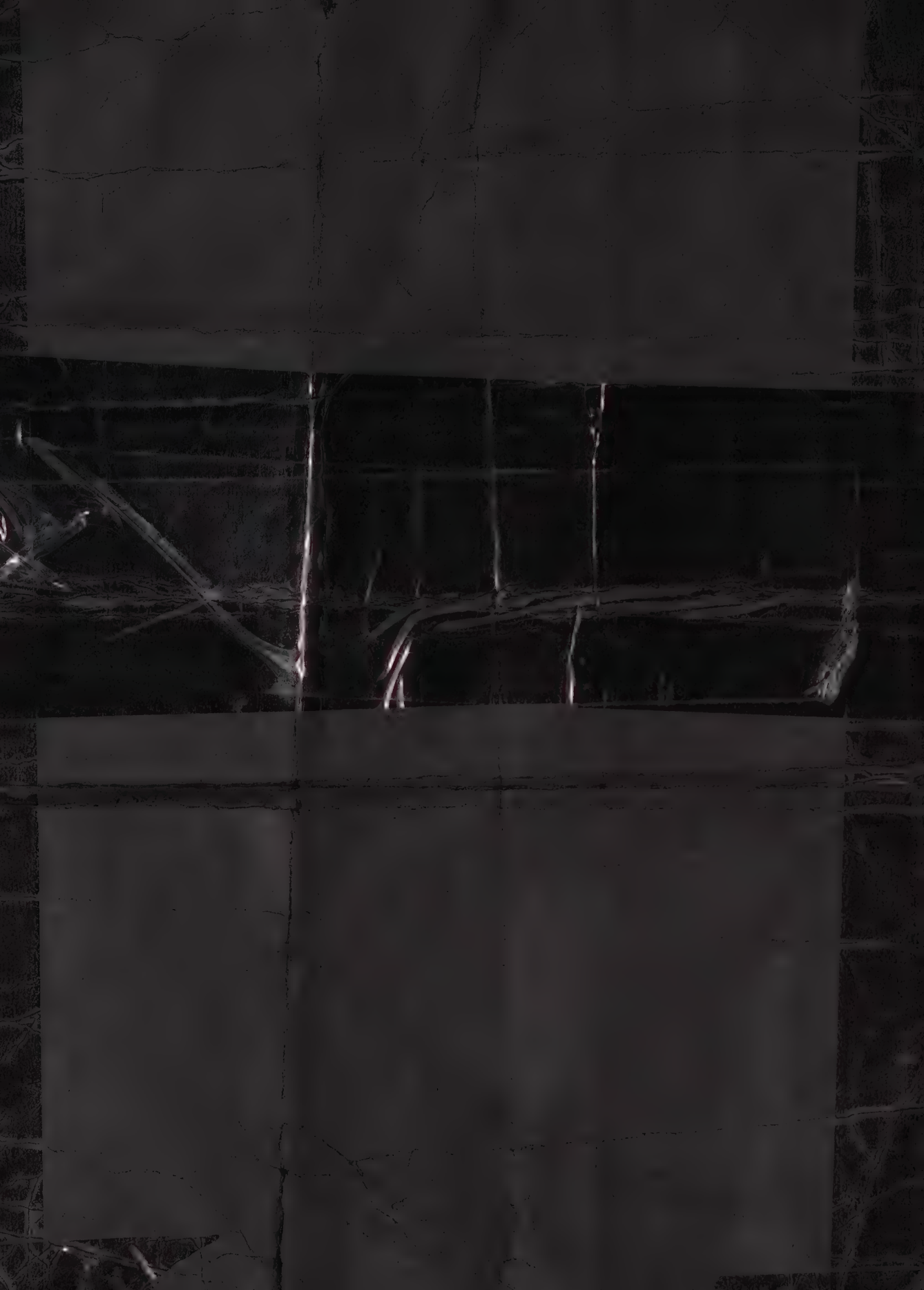
6. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. .5msec/div.
   Trigger: Int CH 1
   1015: Display Mode CH 1-4 VST

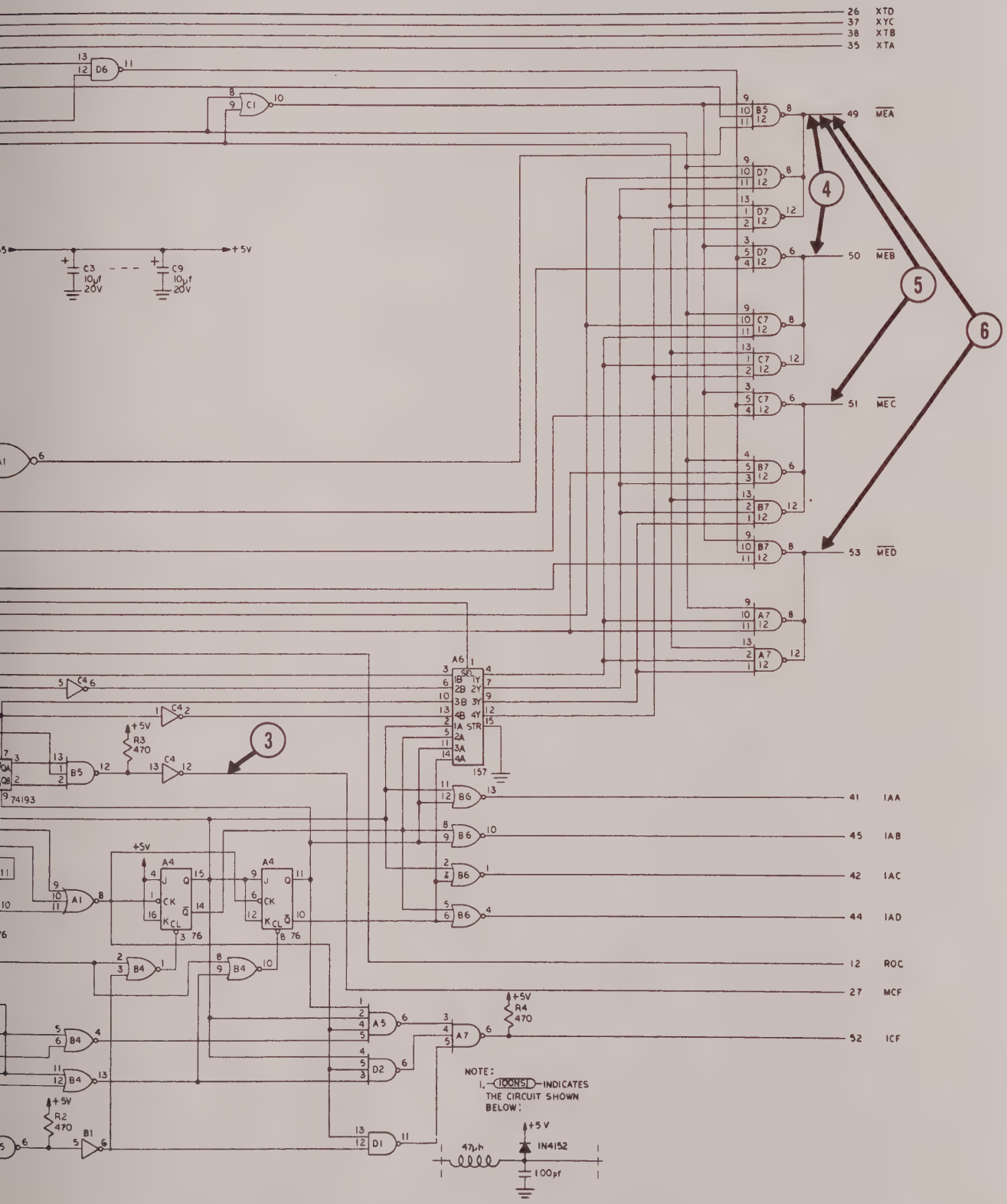


7. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. .5μsec/div.
   Trigger: Int on CH 2 ICF
   1015:

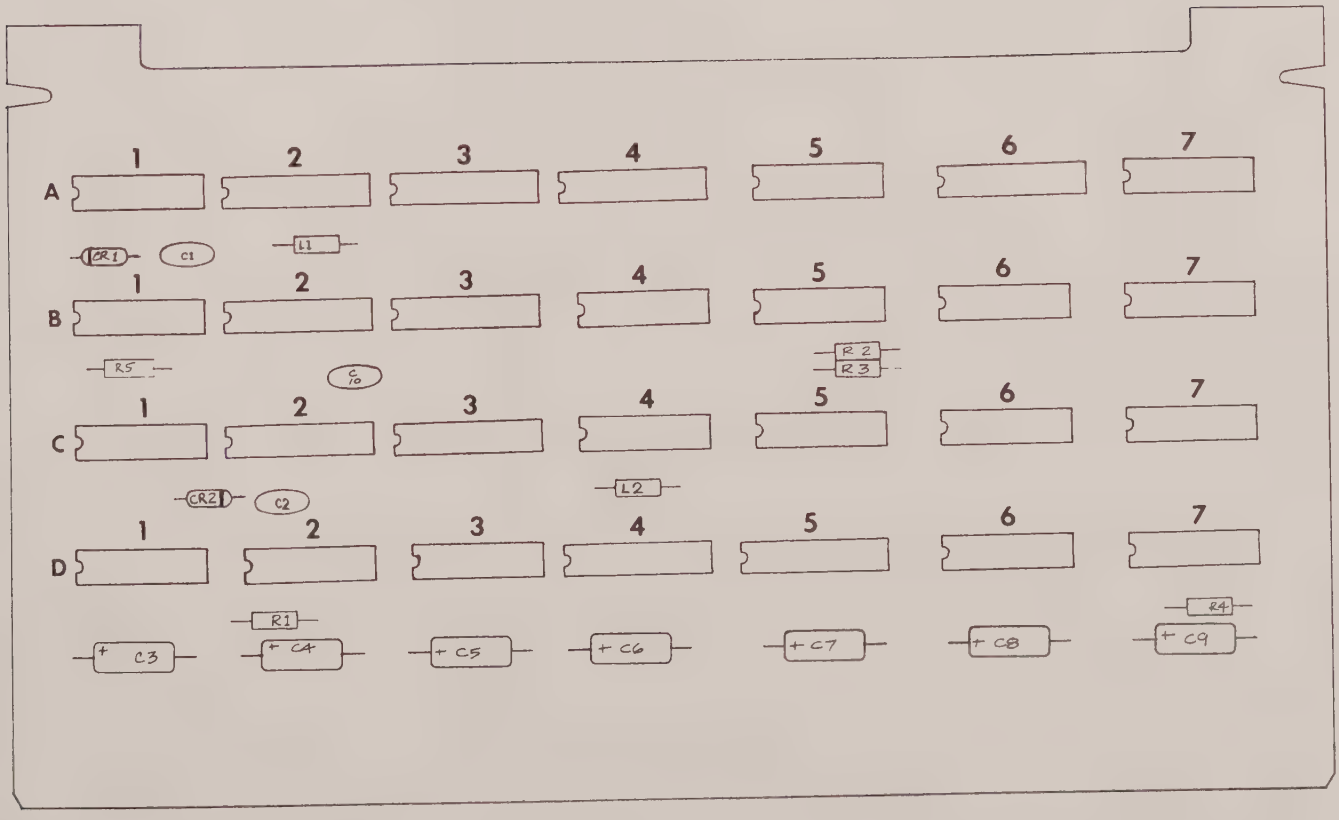

ASB 46
ASA 43
EOP 14
EOO 21
PLT 19
DIG 17
XCK 47
XCK 24
XCL 48
XCL 25
OPT 13
AWH 16
CCD 18
ICC 20
WRC 22
PTR 33
ADD 34
ABB 36
REC 11
74175
74193
157
100NS
330pf
+5V
1K
R5 100
C10 330pf
8.9.54.



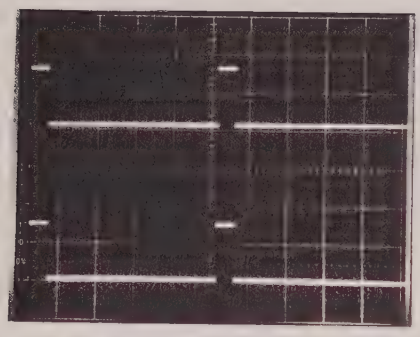




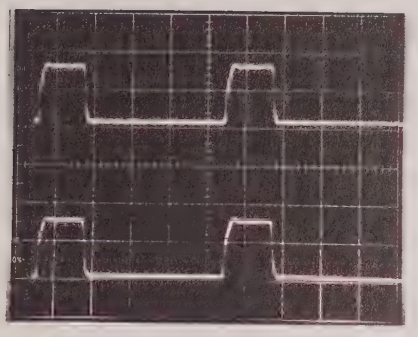
Output Address



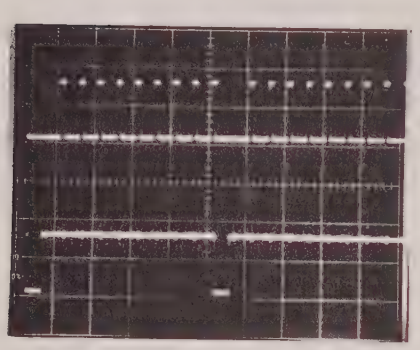
Output Address
-103A-



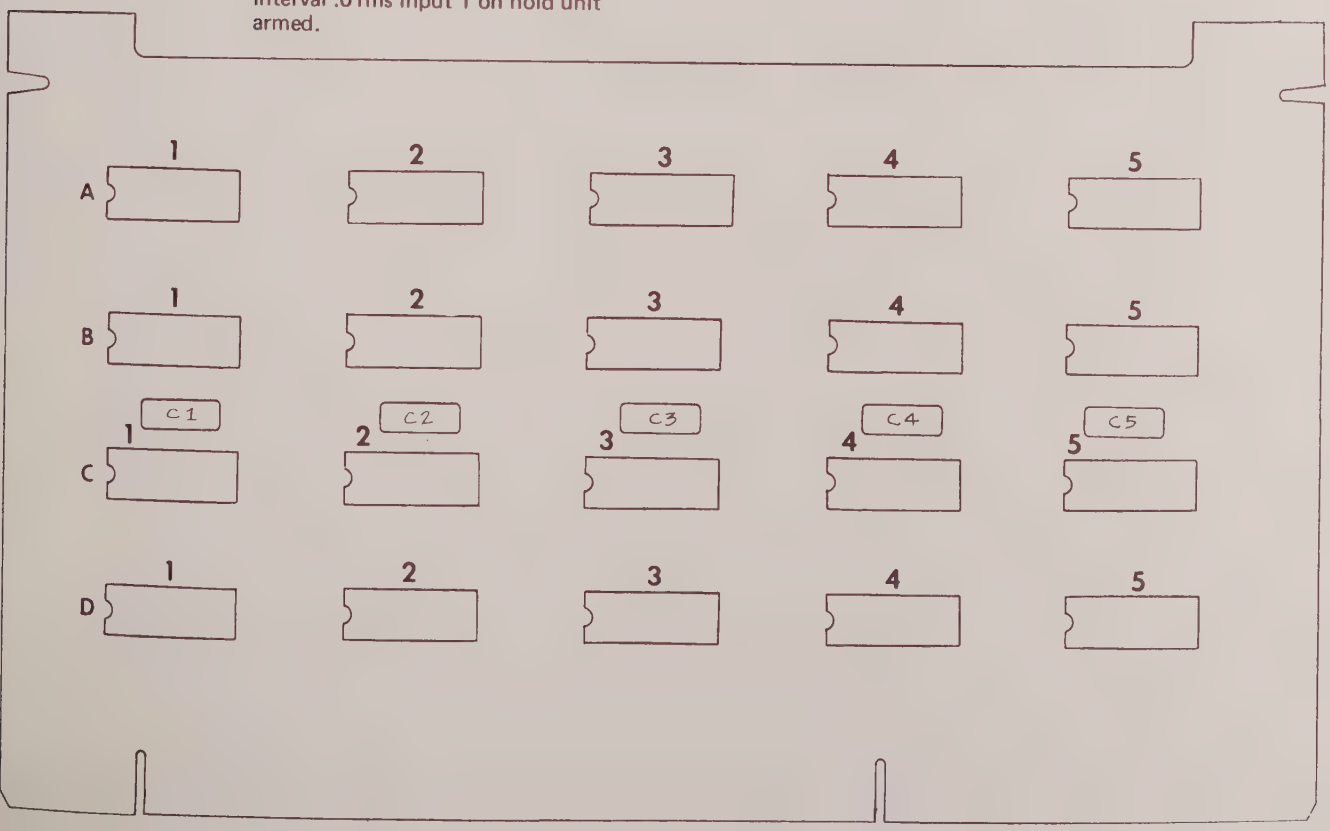
1. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. 2μsec/div
   Trigger: Int CH1
   1015: Auto trigger, sample interval .01ms. Typical MWA, MWB, MWC, MWD.

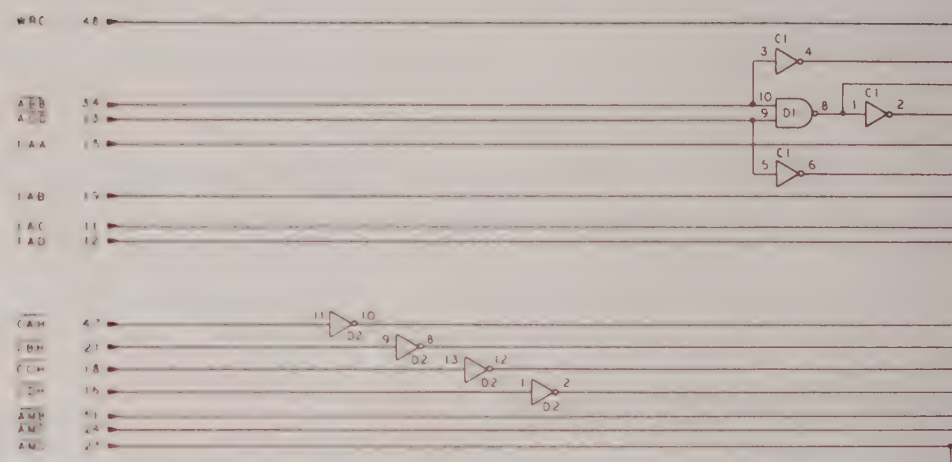


2. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. .2μsec/div
   Trigger: Int CH 1
   1015: Display mode.



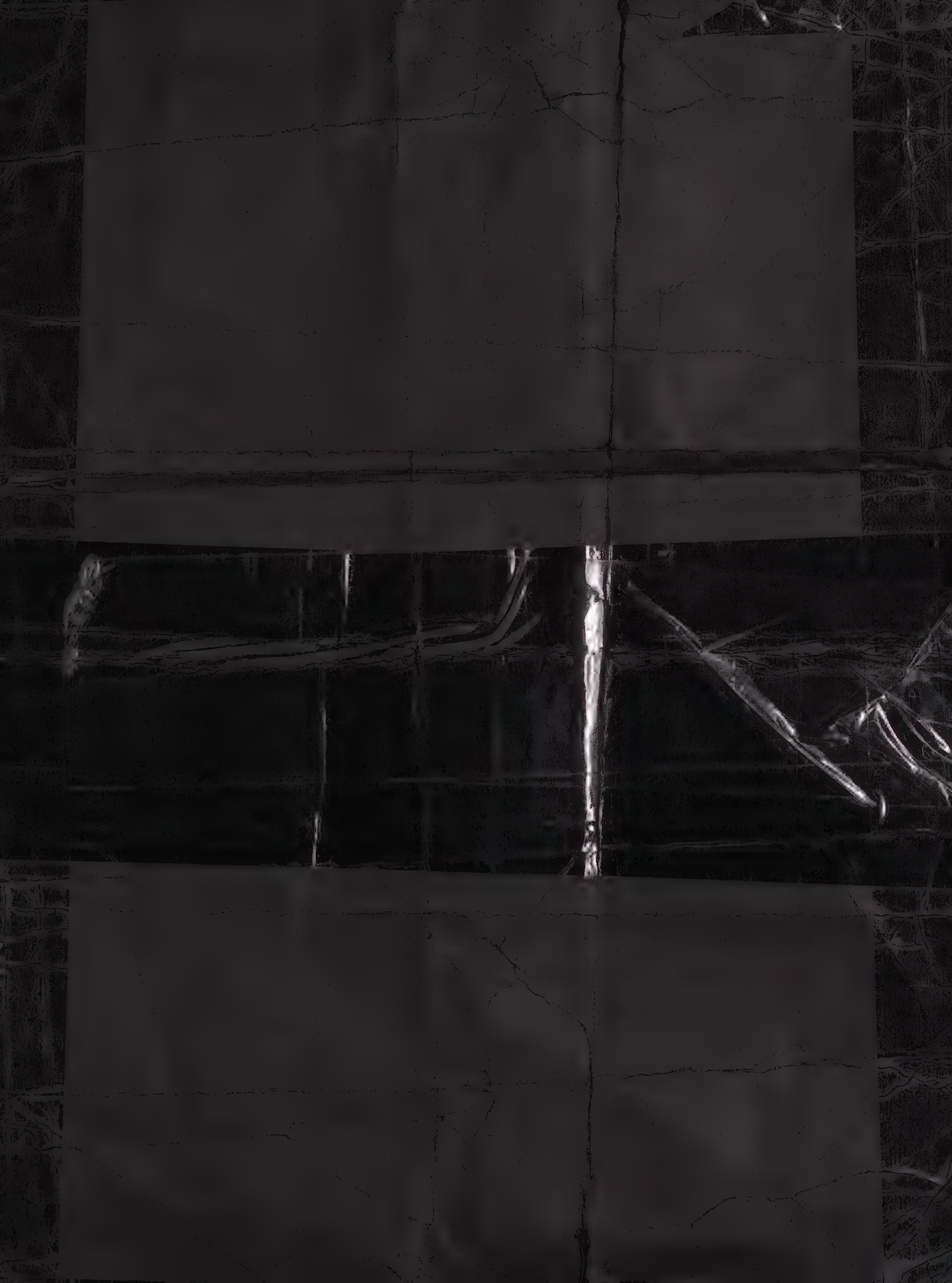
3. Scope: Vert. CH 1 & 2 2 v/div,
   Horz. 2μsec/div
   Trigger: Int CH 2
   1015: Pretrig Record Mode, sample interval .01ms input 1 on hold unit armed.

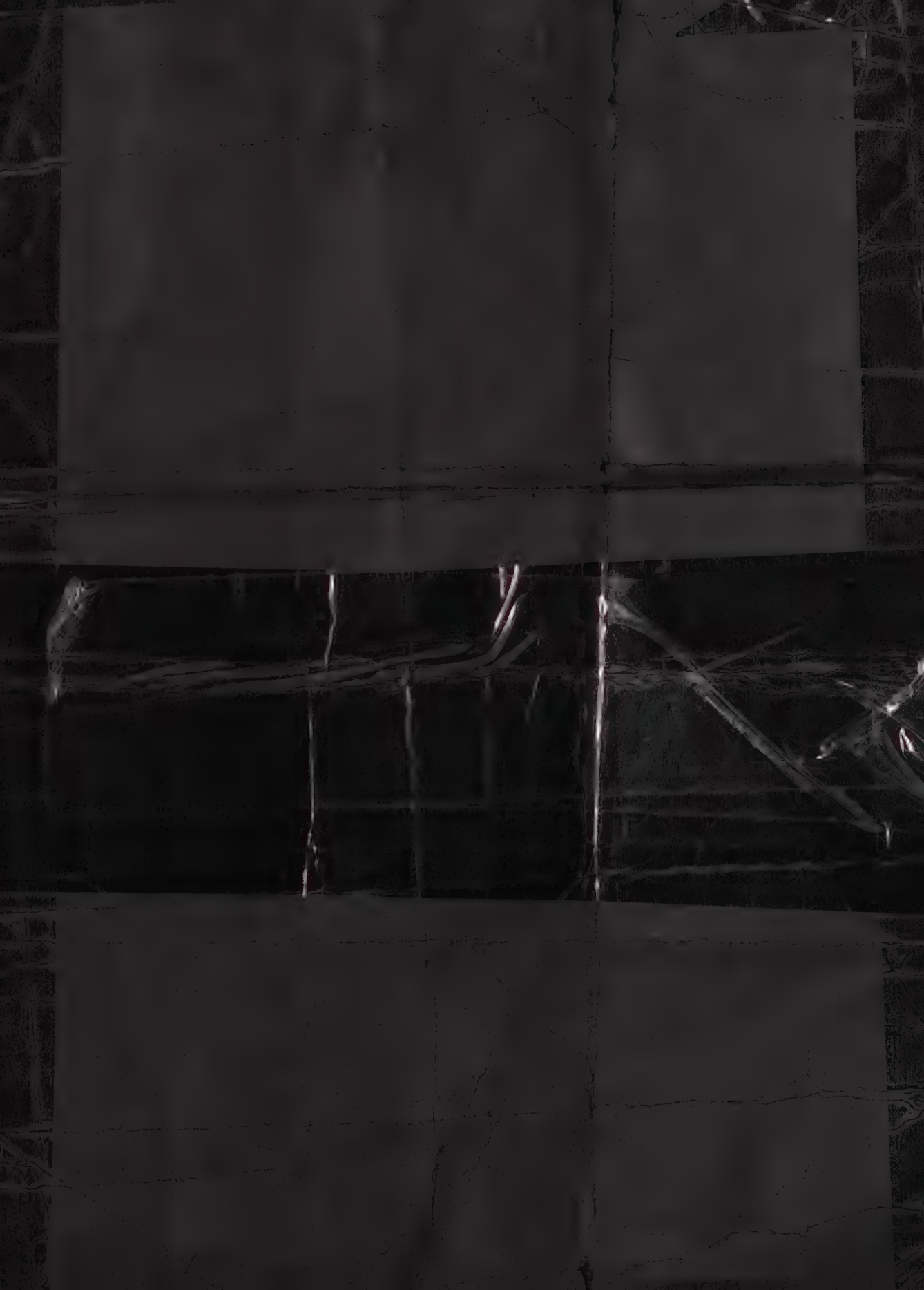


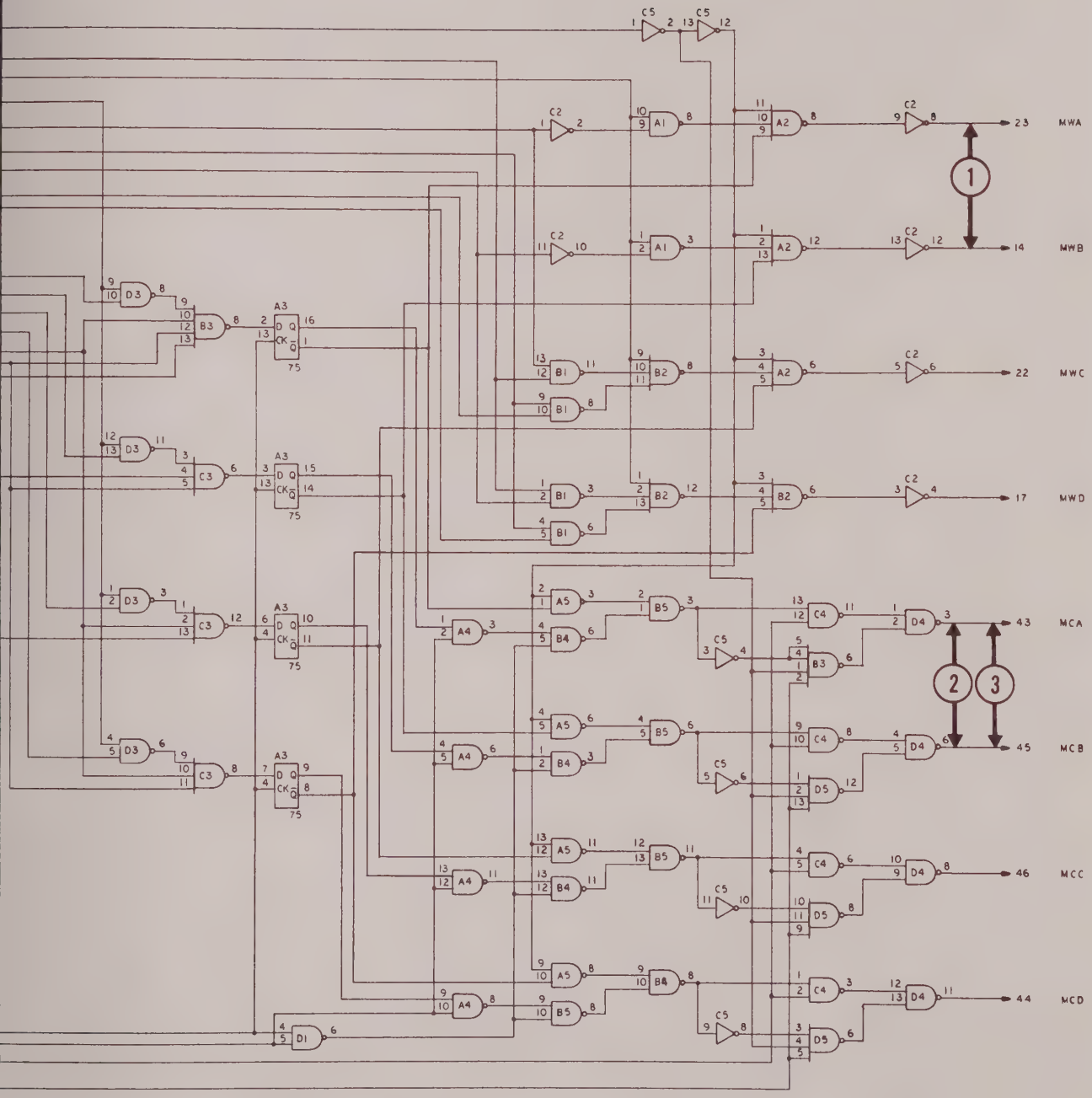

C1
D1
D2

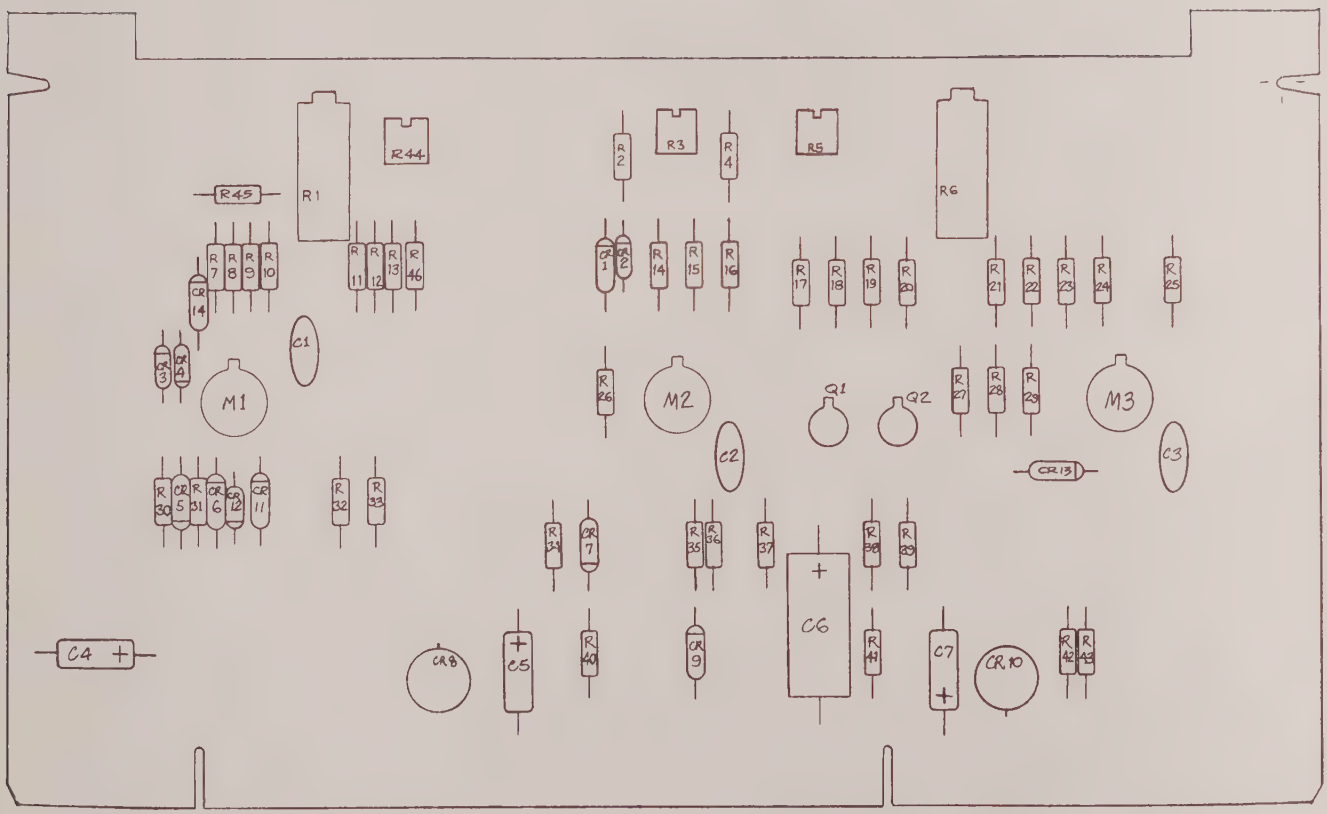
+5V 8,9,54,55
+5V
C1 – C5
10 µf
20V

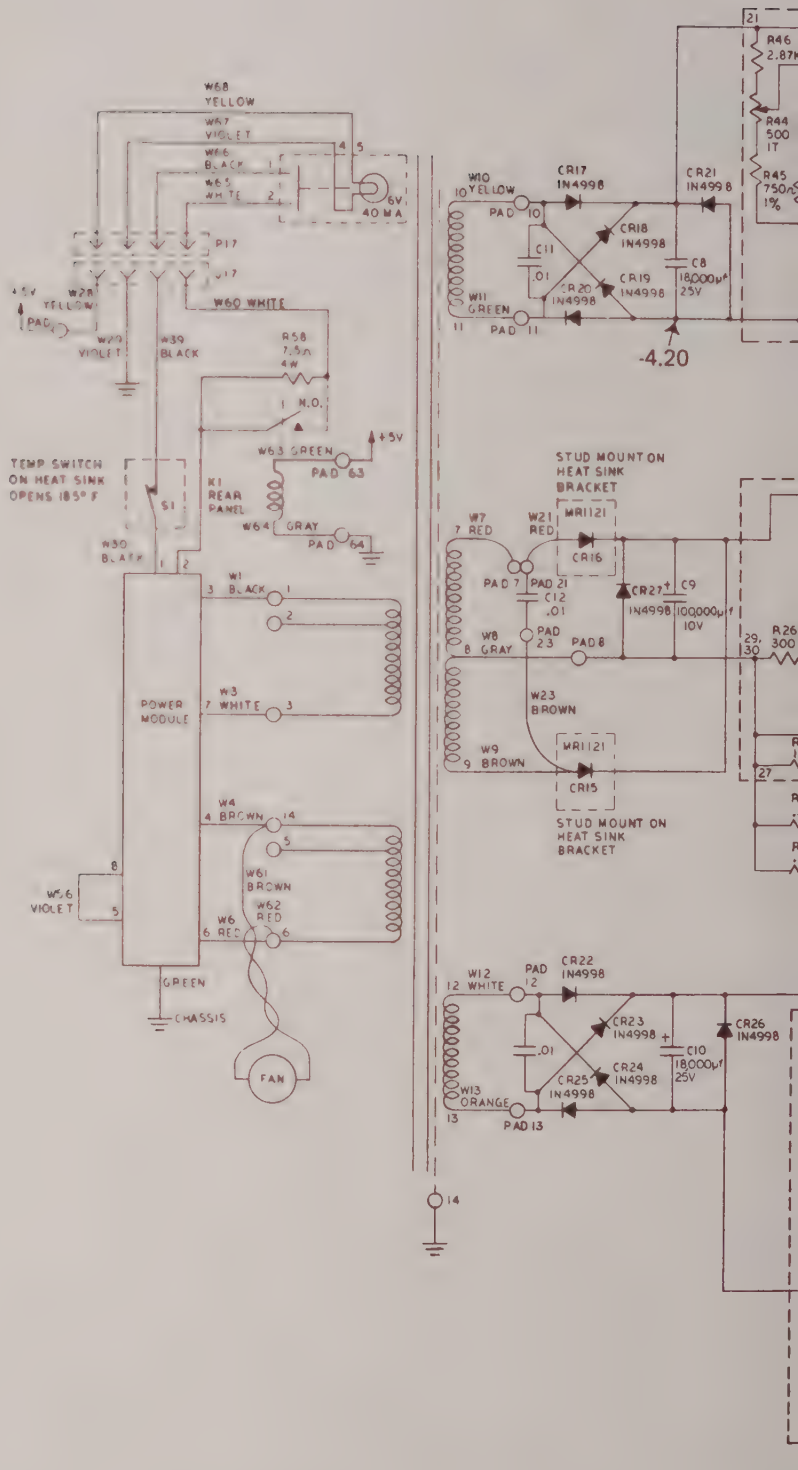
D1
D2



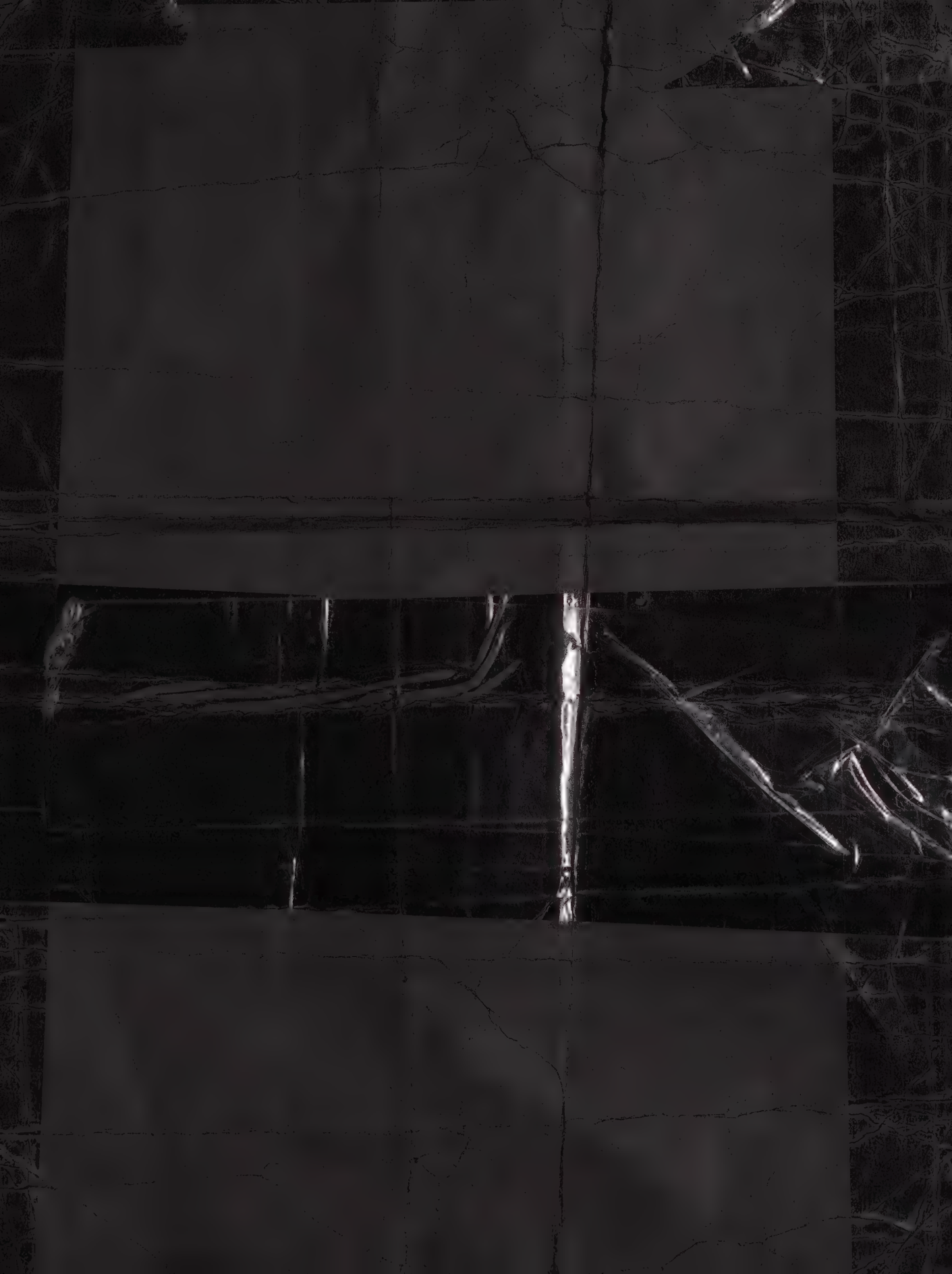


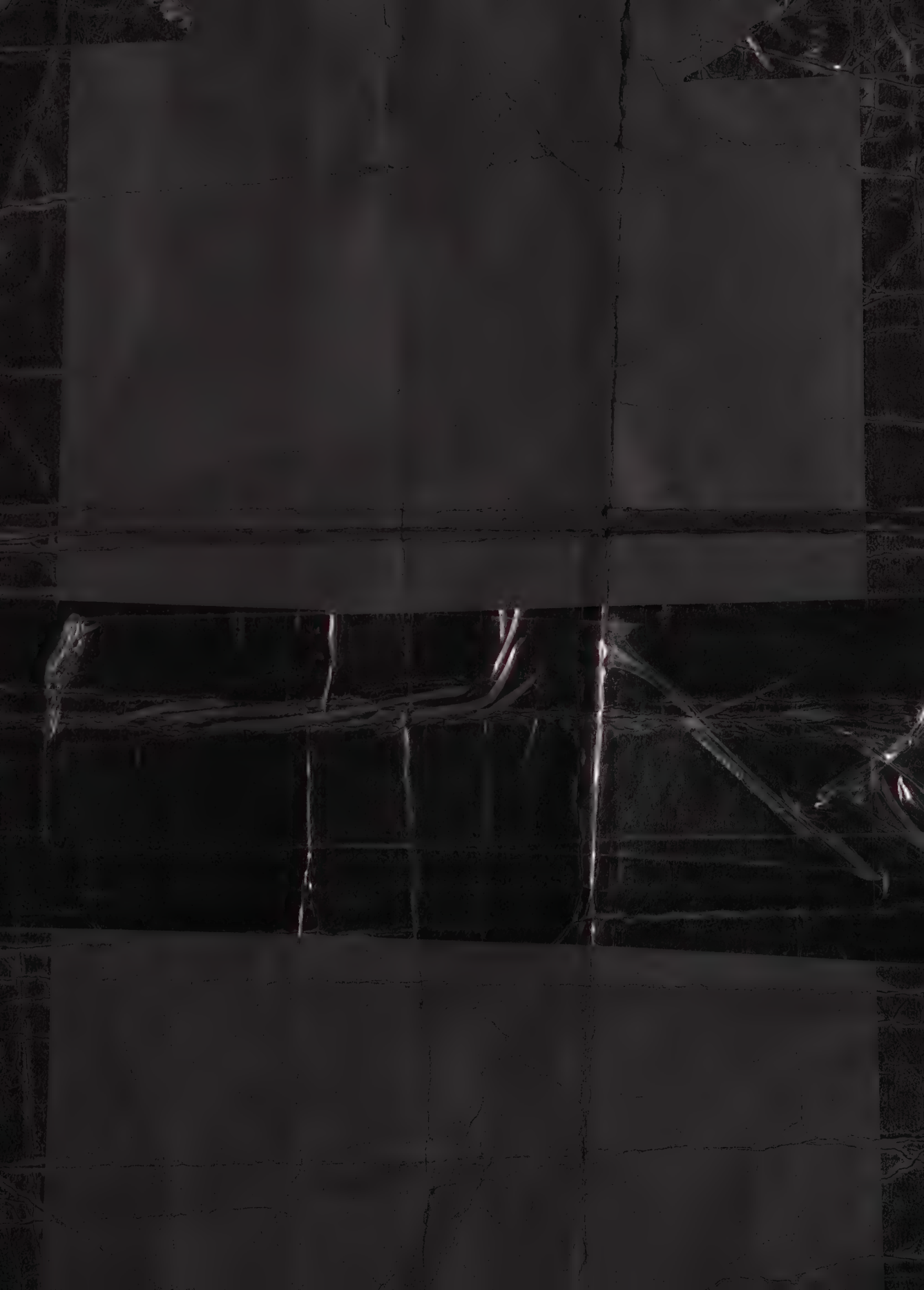

MWA
MWB
MWC
MWD
MCA
MCB
MCC
MCD
A3
D Q
CK Q
75

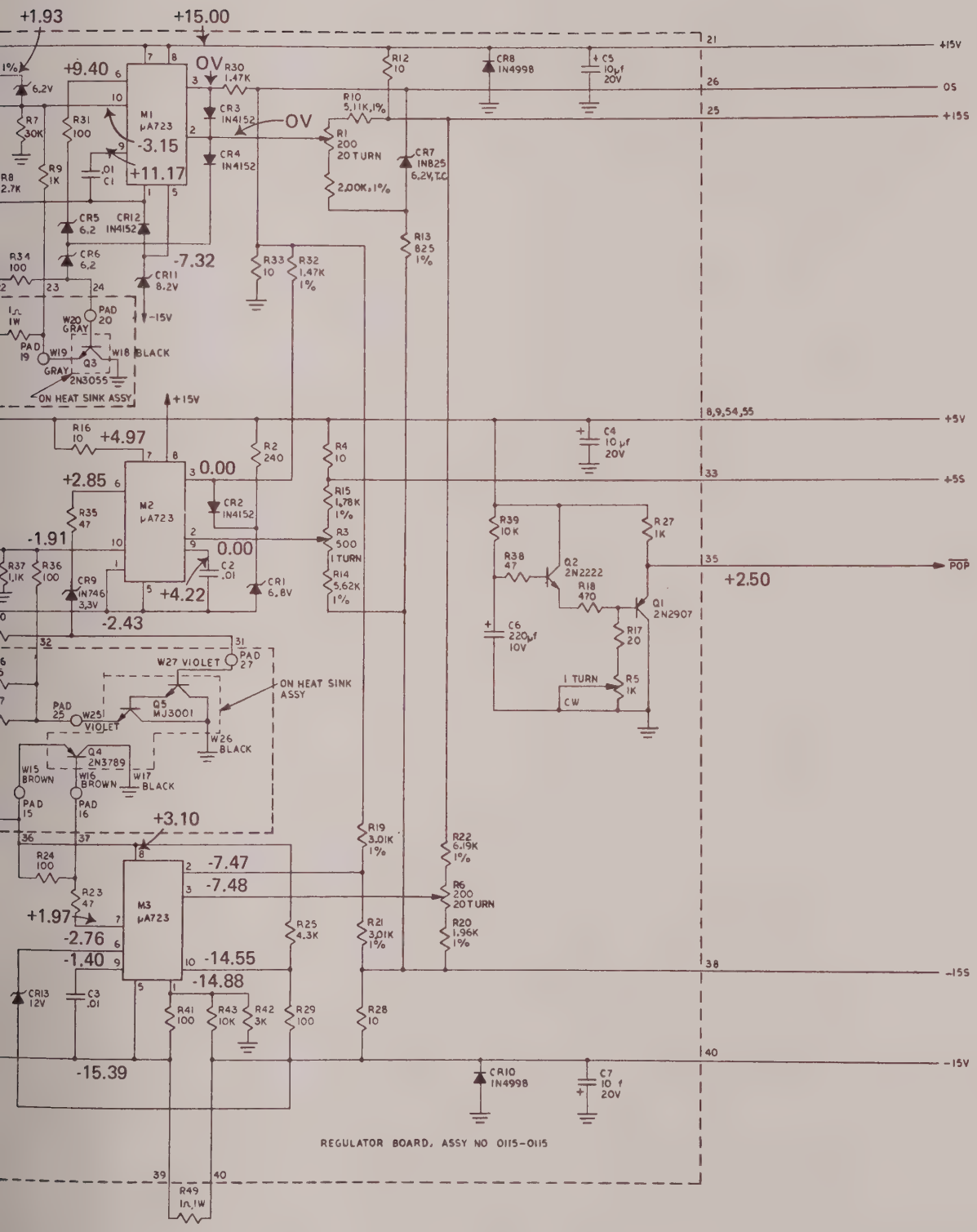

R1
R44
R45
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R46
CR1
CR2
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
CR14
CR3
CR4
C1
M1
R26
M2
Q1
Q2
R27
R28
R29
M3
C2
C3
CR13
R30
CR5
R31
CR6
CR12
CR11
R32
R33
R34
CR7
R35
R36
R37
R38
R39
C4
CR8
C5
R40
CR9
C6
R41
C7
CR10
R42
R43

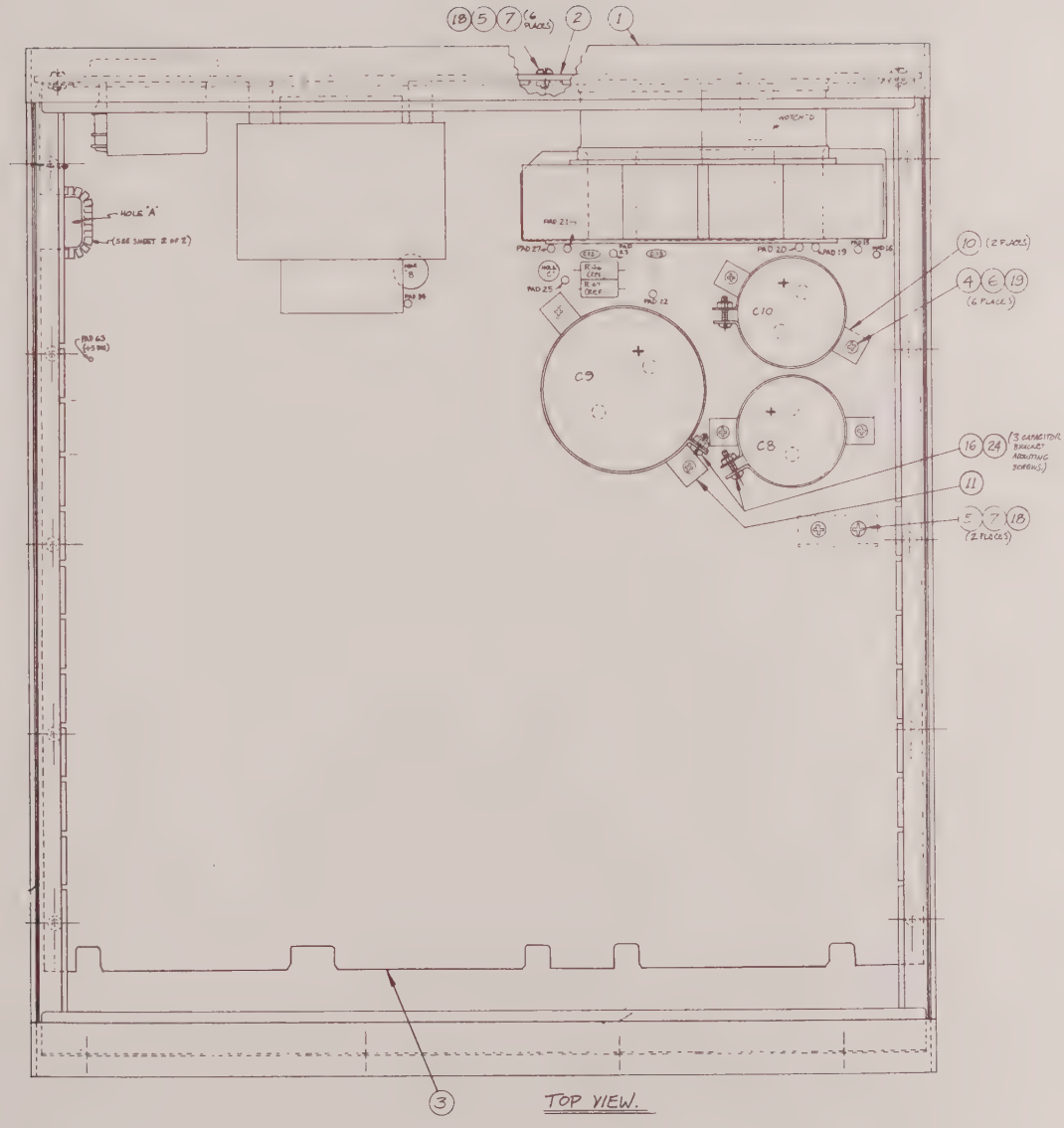


All DC Levels taken with voltmeter Reference to Chassis Ground Line Voltage 110VAC

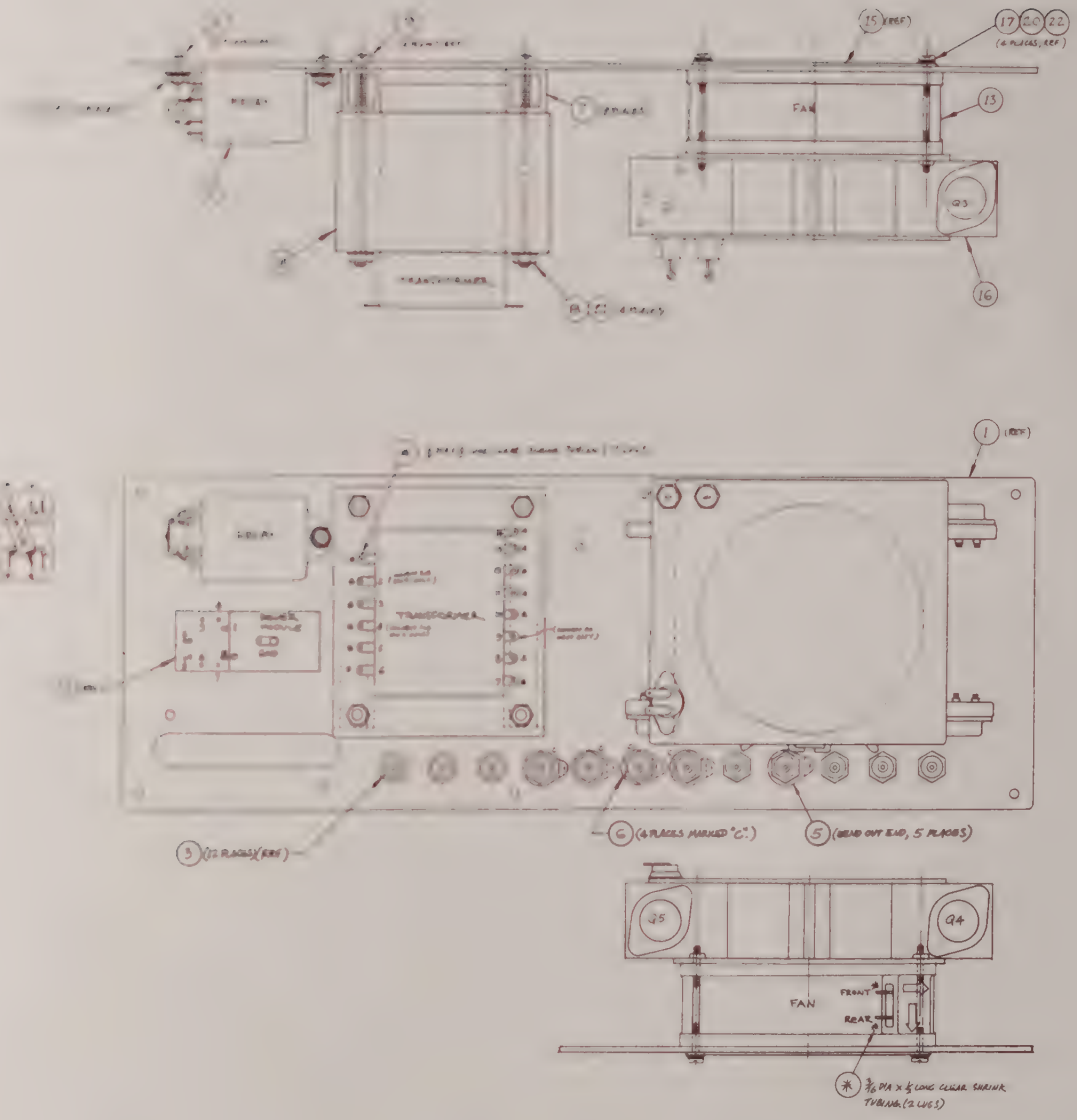


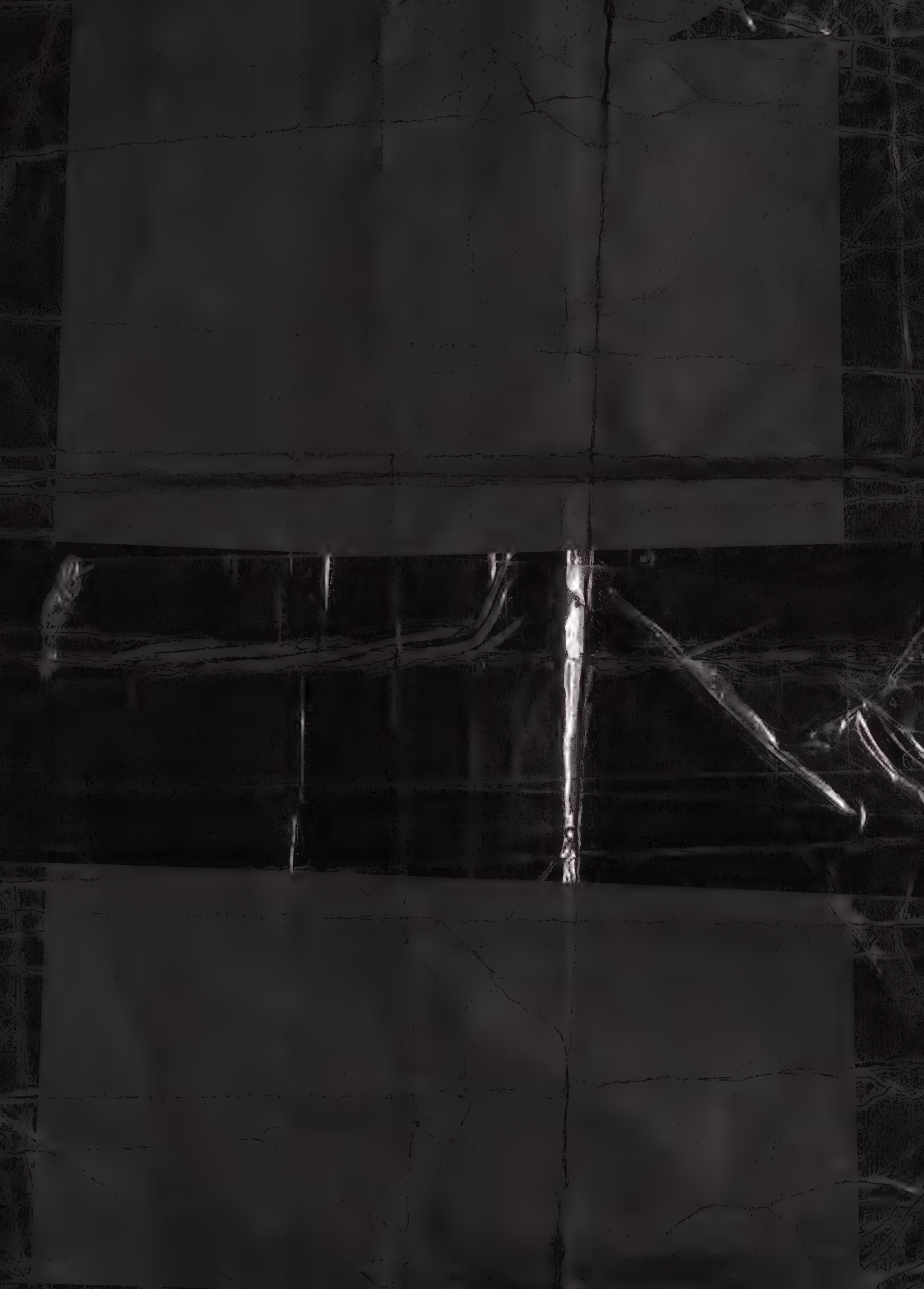


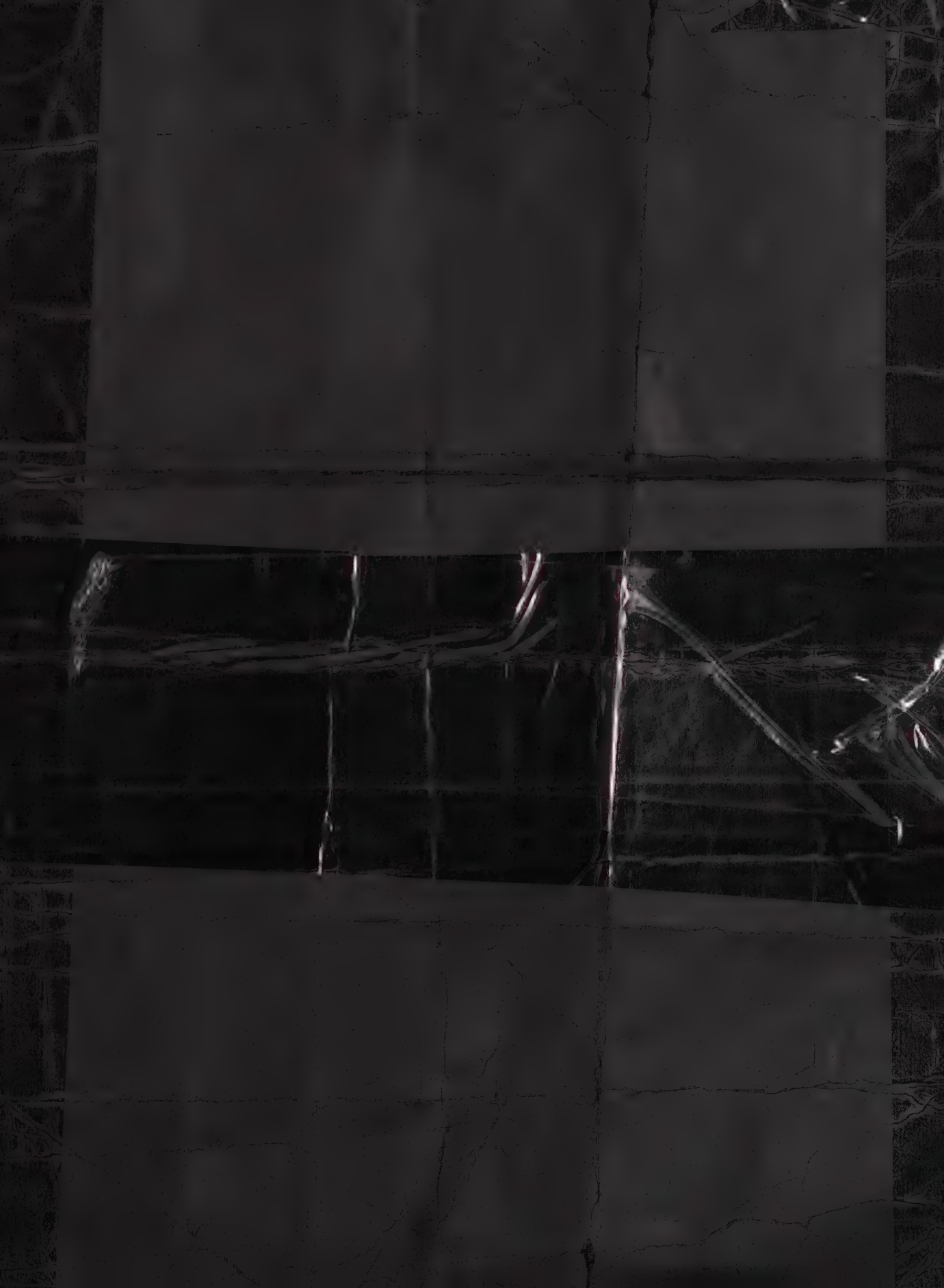

+1.93
+15.00
+9.40
OV
-3.15
+11.17
-7.32
+4.97
0.00
+2.85
-1.91
0.00
+4.22
-2.43
+3.10
-7.47
-7.48
+1.97
-2.76
-1.40
-14.55
-14.88
-15.39
+2.50
M1 µA723
M2 µA723
M3 µA723
R30 1.47K
R12 10
CR8 IN4998
C5 10µf 20V
R10 5.11K,1%
CR3 IN4152
CR4 IN4152
R1 200 20 TURN
2.00K,1%
CR7 IN825 6.2V,TC
R13 825 1%
R33 10
R32 1.47K 1%
CR5 6.2
CR12 IN4152
CR6 6.2
CR11 8.2V
R34 100
W20 GRAY
PAD 20
PAD 19
W19
W18 BLACK
Q3 2N3055
ON HEAT SINK ASSY
R16 10
R2 240
R4 10
C4 10 µf 20V
R15 1.78K 1%
R3 500 1 TURN
R14 5.62K 1%
CR2 IN4152
CR1 6.8V
C2 .01
R35 47
R37 1.1K
R36 100
CR9 IN746 3.3V
R39 10K
R38 47
Q2 2N2222
R18 470
Q1 2N2907
R27 1K
R17 20
C6 220µf 10V
R5 1K
1 TURN CW
W27 VIOLET
PAD 27
Q5 MJ3001
ON HEAT SINK ASSY
PAD 25
W25 VIOLET
W26 BLACK
Q4 2N3789
W15 BROWN
W16 BROWN
W17 BLACK
PAD 15
PAD 16
R19 3.01K 1%
R22 6.19K 1%
R6 200 20 TURN
R20 1.96K 1%
R21 3.01K 1%
R24 100
R23 47
R25 4.3K
CR13 12V
C3 .01
R41 100
R43 10K
R42 3K
R29 100
R28 10
CR10 IN4998
C7 10 f 20V
R49 In.1W
REGULATOR BOARD, ASSY NO 0115-0115
+15V
OS
+15S
+5V
+5S
POP
-15S
-15V
8,9,54,55
21
26
25
33
35
38
40
39

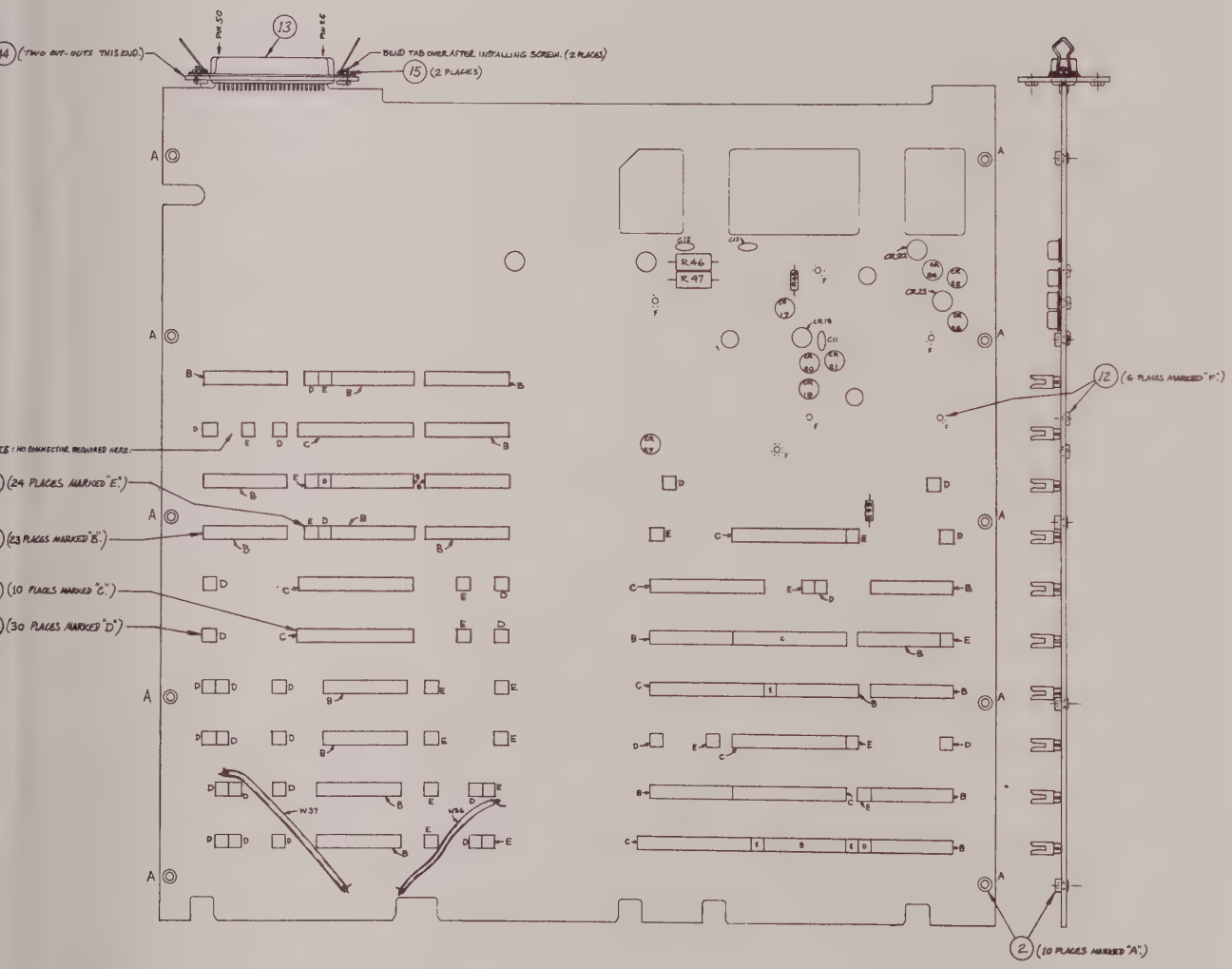

18 5 7 (6 PLACES)
2
1
HOLE 'A'
(SEE SHEET 2 OF 2)
PAD 63
(63 DIA)
PAD 21
PAD 27
PAD 20
PAD 19
PAD 25
PAD 12
C9
C10
C8
10 (2 PLACES)
4 6 19
(6 PLACES)
16 24 (3 CAPACITOR BALLAST ADJUSTING SCREWS)
11
5 7 18
(2 PLACES)
3

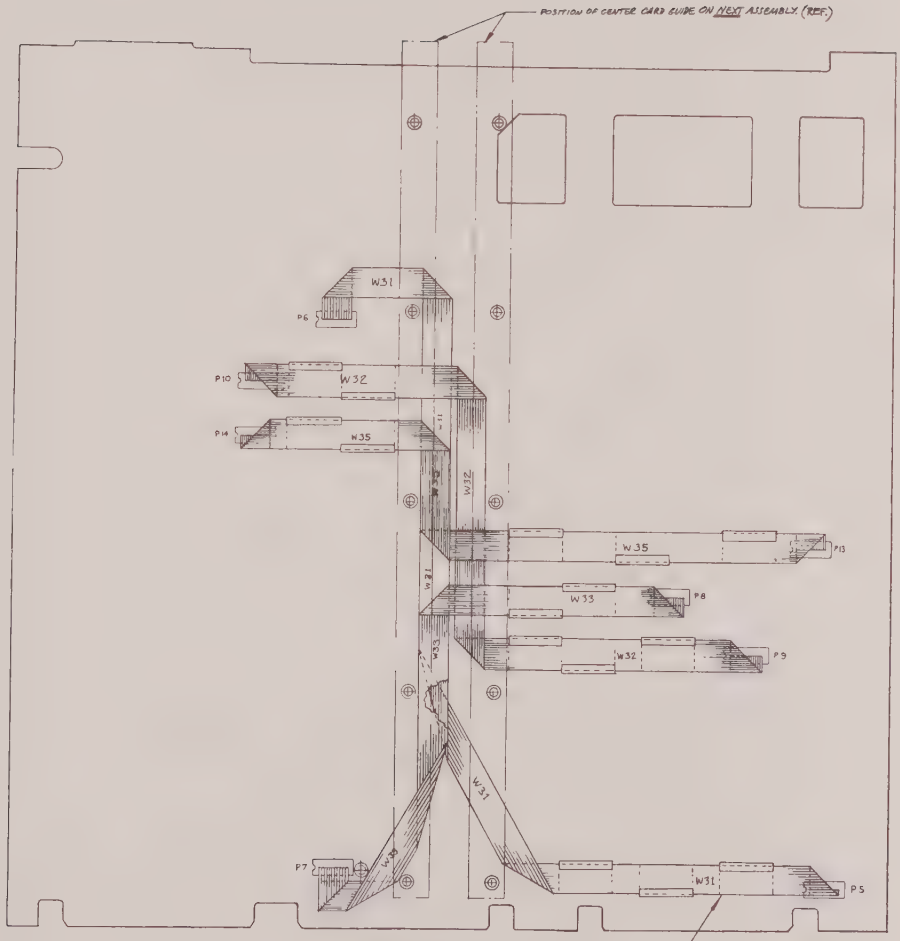
TOP VIEW.


FAN
TRANSFORMER
FAN
FRONT
REAR





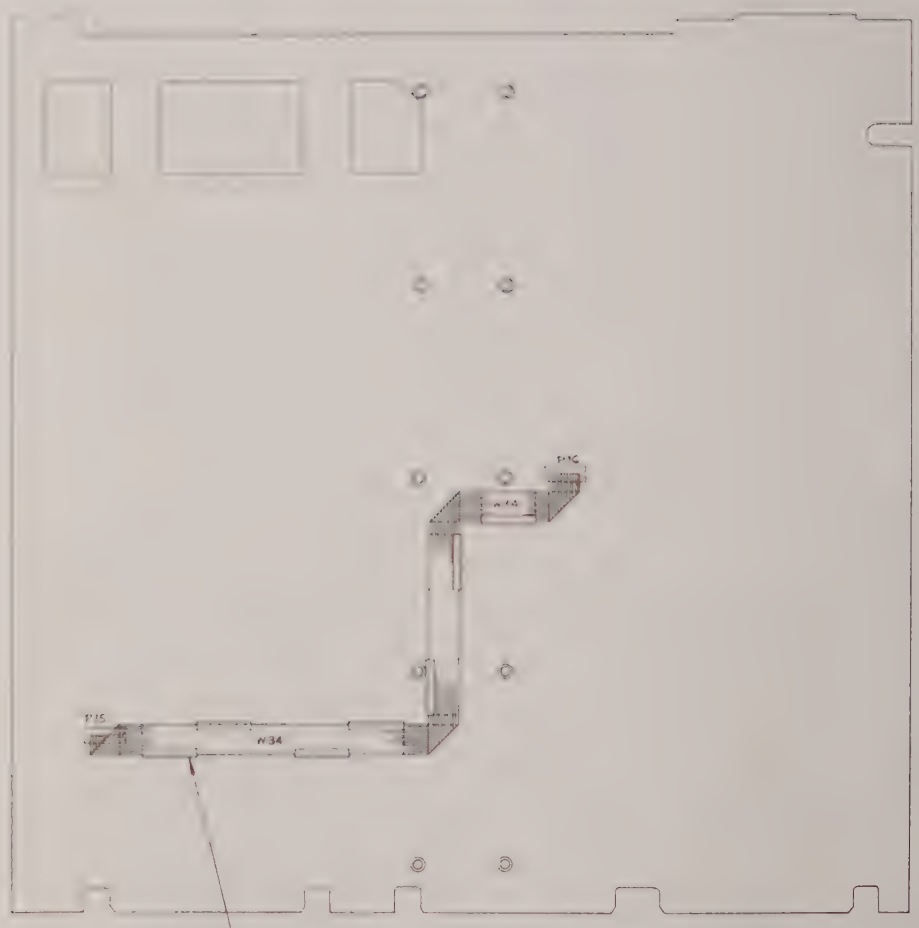

(TWO CUT-OUTS THIS END.)
PW 50
13
PW 86
BEND TAB OVER AFTER INSTALLING SCREW. (2 PLACES)
15 (2 PLACES)
12 (6 PLACES MARKED "F.")
(24 PLACES MARKED "E.")
(23 PLACES MARKED "B.")
(10 PLACES MARKED "C.")
(30 PLACES MARKED "D")
2. (10 PLACES MARKED "A.")
R46
R47
W37
W36



TOP VIEW OF BOARD

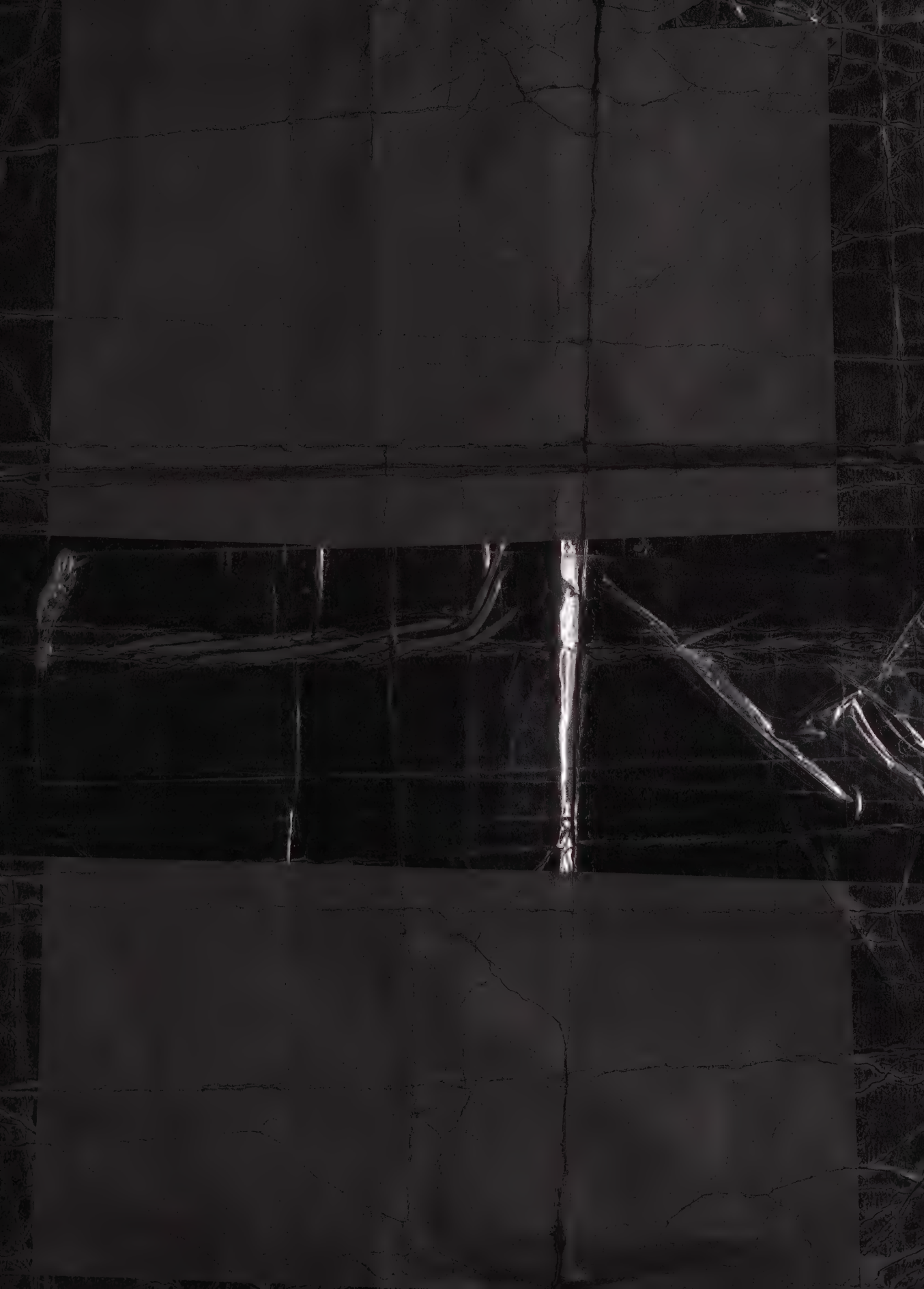
29 (16 PLACES THIS SIDE.)

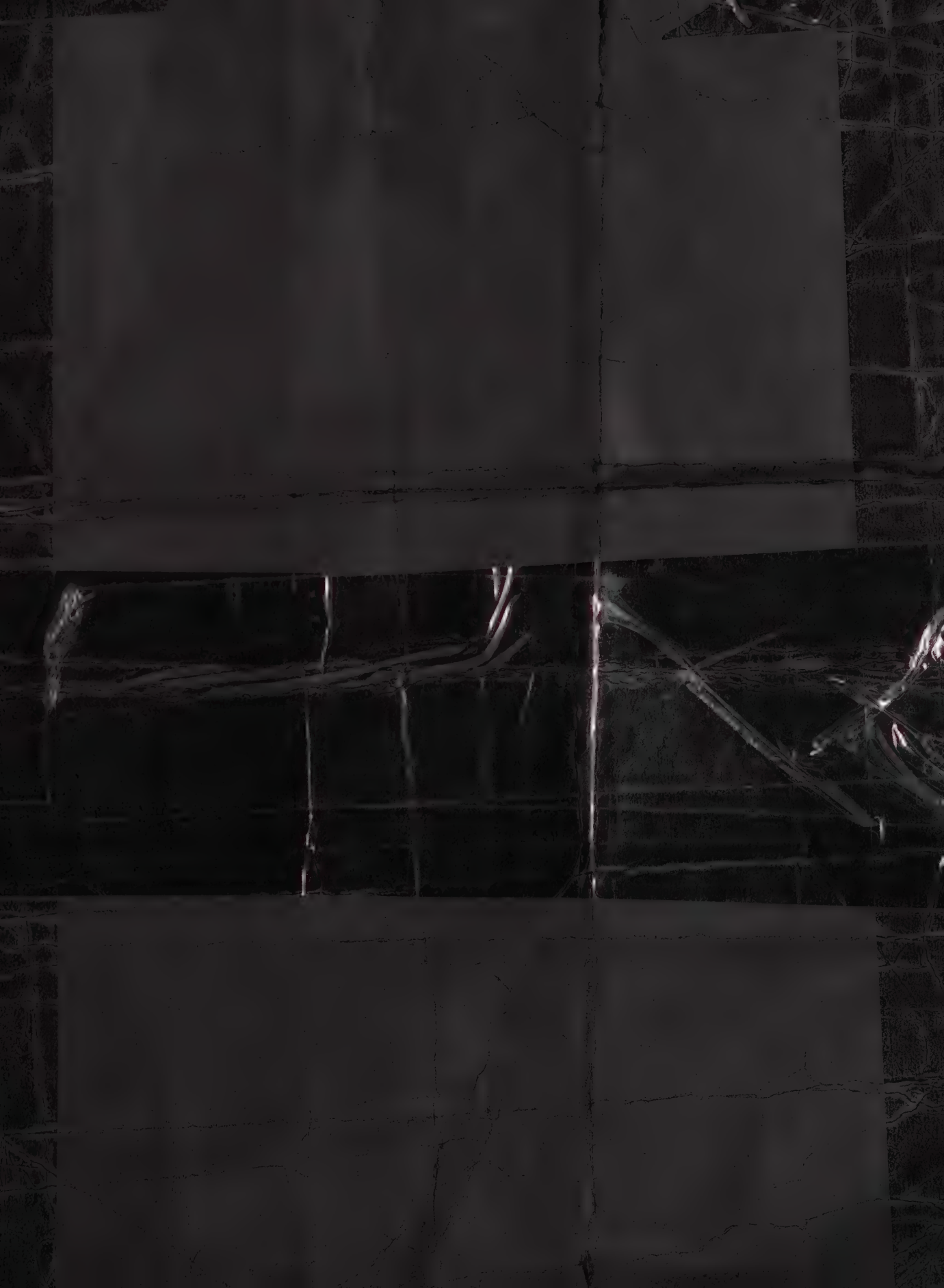
NOTE: SEE SHEET 4 OF 4 FOR W34.

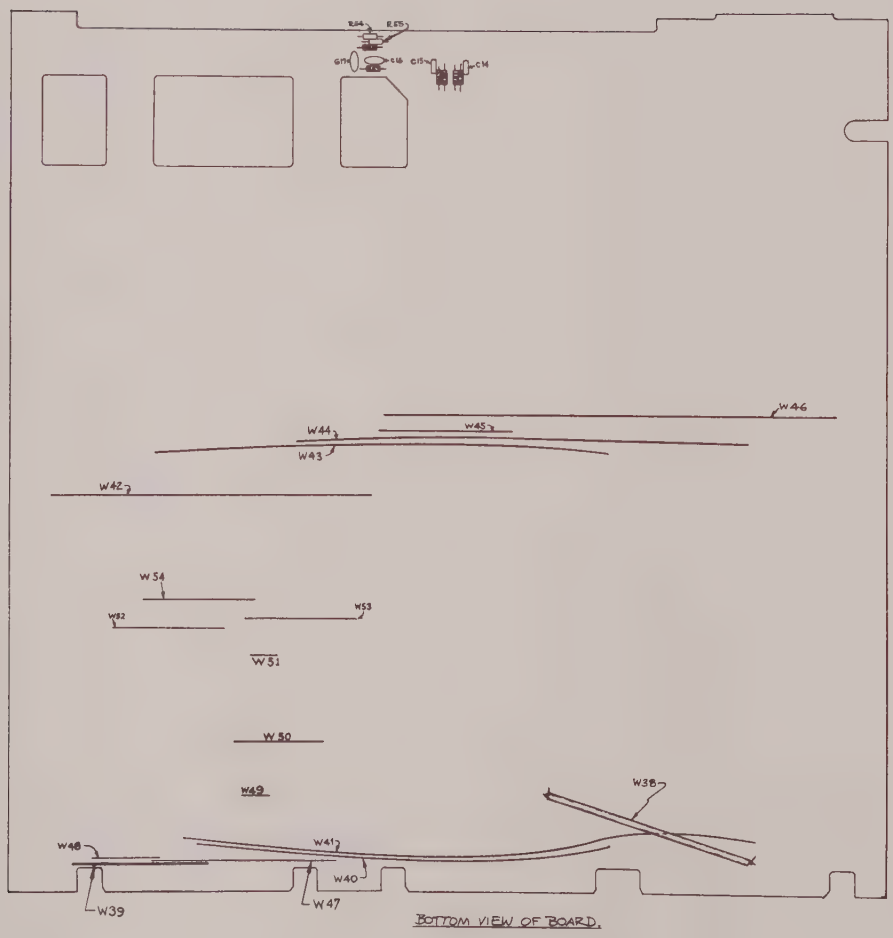


BOTTOM VIEW OF BOARD.

(29) (7 PLACES THIS SIDE OF BOARD.)







BOTTOM VIEW OF BOARD.

SECTION 10

This section contains a complete list of 1015 inter connections with origin and termination points. Also contained in this section is the complete list of Mnemonics and descriptions.

1015 INTERCONNECTION TABLE

Mnemonic	Description	Origin	Termination
AAI	CH1 Input Amp In	Front Panel P1/A	1 & 2 Input Amp Card Pin 6
AAO	No. 1 Amp Output	Input Amp Bd Pin 26	1 A/D Input, Pin 15 Front Panel (2 plcs) P2/P, P1/C
ABB	CH 1&2 only (2048) Input Mode	Front Panel	Record Cont Pin 38; Mem Cont Pin 34; Output Addr Pin 36
ABO	No. 2 Input Amp Output	No. 1&2 Input Amp Bd Pin 30	No. 2 A/O Input, Front Panel (2 plcs) Pin 32 P1/M, P2/13
ABT	CH 1&2 (2048) vs times output SW	F Panel P3/21	Output Addr Bd Pin 31
ACO	No. 3 Input Amp Out	No. 3&4 Input Amp Card Pin 26	No. 3 A/D Input Pin 15 Front Panel (2 plcs) P1/20, P2/N
ADA	Device Address, Digit #1	R Panel 50 Pin Conn, Pin 14	Y DAC Bd Pin 14 Front
ADB	Device Addr, Digit H2	R Panel Conn, Pin 15	Y DAC Bd Pin 12 Front
ADC	Device Address, Bit #3	R Panel Conn Pin 16	Y DAC Bd Pin 6 Front
ADJ	#1 1st stage-10	F Panel P1/2	# 1&2 Input Bd Pin 23
ADM	Auto Digital Mode SW	F Panel P3/V	Output Cont Bd Pin 17
ADO	#4 Input Amp Out	# 3&4 Input Amp Card Pin 30	#4 A/D Input Pin 32; Front Panel (2 plcs) P2/3, P2/12
ADT	Ch 1-4 vs time Output SW	Front Panel P3/18	Output Addr Bd Pin 28
AGD	Analog Ground from Front Panel (Trigger)	Front Panel Pin 2/Z to Dig GND & Other Analog GNDS Just Behind the Channel 3&4 A/D Bd	

Mnemonic	Description	Origin	Termination
AIO	#1 Input Offset Voltage	Front Panel (Pot) P1/F	#1&2 Input Amp Cd Pin 27
AMB	CH1 to Mem 2 (1024) Input Mode	F Panel (Button P2/E	Rec Cont Bd Pin 49; Mem Cont Bd Pin 51
AMC	#1 to #3 Mem Input Mode	F Panel (Button) P2/7	Rec Cont Bd Pin 50; Mem Cont Bd Pin 24
AMD	#1 to #4 Mem Input Mode	F Panel (Button) P2/F	Rec Cont Bd Pin 51; Mem Cont Bd Pin 25
AMH	1 MHZ Clock (75-25 Duty Cycle)	Time Base Bd Pin 34	Rec Cont Bd Pin 17; Mem Cont Bd Pin 52; Output Cont Bd Pin 32; Output Addr Bd Pin 16; X DAC Bd Pin 36; Y DAC & IO Bd Pin 32
AOD	Ch1 (4096) Input Mode	Front Panel (Button) P2/4	Rec Cont Bd Pin 41; Mem Cont Bd Pin 13; Output Addr Pin 34
AOO	CH1 Output Off	F Panel P3/14	Y DAC & Bd Pin 42
AOT	CH1 Only (4096) vs time Output SW	F Panel P3/20	Output Addr 30 Pin 29
APA	Device Addr Polarity, Bit #3	R Panel Conn Pin 22	Y DAC Bd Pin 9 Front
APB	Device Addr Polarity, Bit #2	R Panel Conn Pin 21	Y DAC Bd Pin 10 Front
APC	Device Addr Polarity, Bit #3	R Panel Conn Pin 22	Y DAC Bd Pin 9 Front
ARL	Arm ready Lamp Arm 6	Trig & Cont Bd Pin 12	F Panel P2/X
ASA	Mem Addr Strobe #1	Time Base Bd Pin 21	Output Cont Bd Pin 43; Out Addr Bd Pin 43; Y DAC & IO Bd Pin 31
ASB	Mem Addr Strobe #2	Time Base Bd Pin 18	Out Addr Bd Pin 46
ATR	Auto Trigger Mode	F Panel (Button) P2/21	Trig & Cont Bd Pin 15
AVP	#1 Output Vert Position	F Panel (Pot) P3/6	Y DAC & IO Bd Pin 48
AXA	#1 1st Stage X 1	F Panel (TTL) P1/B	#1&2 Input Bd Pin 22

Mnemonic	Description	Origin	Termination
AXE	#1 2nd Stage x 5	F Panel P1/3	#1&2 Input Bd Pin 24
AXJ	Ch1 2nd State x 10	F Panel P1/N	#1&2 Input Bd Pin 25
BAI	#2 Input Amp In	F Panel P1/9	#1&2 Input Card Pin 49
BDJ	#2 1st Stage ÷ 10	F Panel P1/K	#1&2 Input Bd. Pin 33
BIO	#2 Input Offset	F Panel (POT) P1/5	#1&2 Input Amp Card Pin 29
BLA	Blank 1 (Blanks for Channels turned off)	Y DAC Bd Pin 46F	Out Cont Pin 22
BLB	Blank 2 (Pre-Buffer Z Out)	Y DAC Bd Pin 35	Output Cont Bd Pin 46
BOO	#2 Output off SW	F Panel P3/15	Y DAC & IO Bd Pin 42F
BVP	#2 Output Vert Pos	F Panel (Pot) P3/7	Y DAC & IO Bd Pin 49
BXA	#2 1st Stage x 1	F Panel P1/14	#1&2 Input Bd Pin 34
BXG	#1&2 2nd Stage x 5	F Panel (TTL) P1/12	#1&2 Input Bd Pin 32
BXJ	#2 2nd Stage x 10	F Panel (TTL) P1/2	#1&2 Input Bd Pin 31
CAA	#1 Converter Data Addr	Rec Cont Pin 48	#1&2 Ctr/Mux Bd Pin 25
CAB	#2 Converter Data Addr	Rec Cont Pin 52 52	#1&2 Ctr/Mux Bd Pin 26
CAC	#3 Converter Data Enable	REc Cont Bd Pin 44	#3&4 Ctr/Mux Bd Pin 25
CAD	#4 Converter Data Addr	Rec Cont Bd Pin 43	#3&4 Ctr/Mux Bd Pin 26
CAG	CH1 Ground	Motherboard OS Spot	F Panel P1/1; #1-2 Input Cd; #1&2 A/D Cd Pin 6,7
CAH	#1 Hold	F Panel (push button) P1/5	Mem Cont Cd Pin 47
CAI	#3 Input Amp In	F Panel P1/17	#3&4 Input Bd Pin 6

Mnemonic	Description	Origin	Termination
CBG	Channel 2 Gnd	Motherboard OS Spot	F Panel Pl/8; 1&2 A/D Bd Pin 33, 34; 1&2 Input Bd Pin 46, 47, 48
CBH	#2 Hold	F Panel (Push Button) Pl/6	Mem Cont Cd Pin 21
CCD	Mem Ctr Clock Disable	Output Cont Bd Pin 52	Output Addr Bd Pin 18
CCE	Convert Command Enable	Trigger & Cont Bd Pin 23	Rec Cont Bd Pin 32
CCG	Ch 3 Gnd	Motherboard OS Spot	F Panel Pl/V; #3&4 Input Cd; #3&4 A/D Cd Pin 6,7
CDH	#4 Hold	F Panel Pl/Z	Mem Cont Bd Pin 16
CDG	Channel 4 Gnd	Motherboard OS Spot	F Panel Pl/21; #3&4 Input Bd Pin 46, 47, 48; #3&4 A/D Bd Pin 33, 34
CCH	CH #3 Hold	F Panel (push button) Pl/16	Mem Cont Cd Pin 18
CDJ	#3 1st Stage	F Panel (TTL) 1/20	#3&4 Input Bd Pin 23
CIO	#3 Input Offset	F Panel (Pot)	#1&4 Input Cd Pin 27
COC	Convert Command	Rec Cont Bd Pin 42	#1&2 A/D Bd Pin 25; #3&4 A/D Bd Pin 25
COO	#3 Output Off	F Panel P3/13	Y DAC & IO Bd Pin 43
CTR	Reclocked Trigger	Trigger & Cont Bd Pin 42	Rec Cont Bd Pin 35
CVP	#3 Output Vert Position	F Panel (Pot) P3/H	Y DAC & IO Bd Pin 48 (F)
CXA	#3 1st stage x 1	F Panel Pl/19	#3&4 Input Bd Pin 22
CXG	#3 2nd Stage x 5	F Panel Pl/W	#3&4 Input Bd Pin 24
CXJ	#3 2nd Stage x 10	F Panel (TTL) Pl/W	#3&4 Input Bd Pin 25
DAA	Delay 10^{-2} Dig, Bit 1 (2°)	F Panel P2/M	Trigger & Cont Bd Pin 26

Mnemonic	Description	Origin	Termination
DAB	Delay 10^{-2} Dig, Bit 2 (2°)	F Panel P2/R	Trigger & Cont Bd Pin 24
DAC	Delay 10^{-2}_{2} Dig Bit 3 (2^{2})	F Panel P2/18	Trigger & Cont Pin 30
DAD	Delay 10^{-2}_{3} Dig Bit 4 (2^{3})	F Panel P2/T	Trigger & Cont Bd Pin 31
DAI	#4 Input Amp In	F Panel P1/22	#3&4 Input Bd Pin 49
DBA	Delay 10^{-1} Dig, Bit 1 (2^{0})	F Panel P2/W	Trigger & Cont Bd Pin 35
DBB	Delay 10^{-1}_{1}Dig, 2nd Bit (2^{1})	F Panel P2/17	Trigger & Cont Bd Pin 34
DBC	Delay 10^{-1}_{2}Dig 3rd Bit (2^{2})	F Panel P2/V	Trigger & Cont Bd Pin 39
DBD	Delay 10^{-1}_{3}Dig 4th Bit (2^{3})	F Panel P2/5	Trigger & Cont Bd Pin 40
DBV	DAC Bias Voltage	Y DAC Bd Pin 40F	X DAC Bd Pin 46
DCA	Delay, 1's$_{0}$Dig, 1st Bit (2^{0})	F Panel P2/V	Trigger & Cont Bd Pin 43
DCB	Delay, 1's$_{1}$Dig, 2nd Bit (2^{1})	F Panel P2/16	Trigger & Cont Bd Pin 41
DCC	Delay, 1's$_{2}$Dig, 3rd Bit (2^{2})	F Panel P2/15	Trigger & Cont Bd Pin 48
DCD	Delay, 1's$_{3}$Dig, 4th Bit (2^{3})	F Panel P2/14	Trigger & Cont Bd Pin 49
DDJ	#4 1st stage ÷ 10	F Panel (TTL) P2/1	#3&4 Input Bd Pin 33
DIC	Digital Interval Command	Out Cont Bd	Mem Cont Bd Pin 10
DIG	Digital Output Command	Output Cont Bd Pin 34	Trigger & Cont Bd Pin 33; Output Addr Bd Pin 17; Y DAC & IO Bd Pin 45
DIO	#4 Input Offset	#Panel (Pot)	#3&4 Input Bd Pin 29
DOB	Digital Output	F Panel P3/Z	Output Cont Bd Pin 15

Mnemonic	Description	Origin	Termination
DOB	Digital Output Pushbutton	F Panel P3/22 Also R.P. Conn Pin 10	Output Cont Bd Pin 11
DOG	Digital Output Command Gated with Device Addr	Y DAC Bd Pin 8 (F)	R Panel 50 Pin Connector Pin 35
DOO	#4 Output Off SW	F Panel P3/R	Y DAC & IO Bd Pin 45 (F)
DES	Data Strobe Enable	Output Cont Bd Pin 51	X DAC Bd Pin 41; Y DAC Bd Pin 33
DTB	Dual Time Base Mode	F Panel (Button) P3/5	Trigger & Cont Bd; Pin 36
DVA	Device Address	Y DAC Bd Pin 15 (F)	Out Cont Bd Pin 20
DVP	#4 Output Vert Pos	F Panel (Pot) P3/J	Y DAC & IO Bd Pin 49
DXA	#4 1st Stage x 1	F Panel (TTL) P2/B	#3&4 Input Bd Pin 34
DXE	#4 2nd Stage x 5	F Panel (TTL) P2/A	#3&4 Input Bd Pin 32
DXJ	#4 Amp 2nd St x 10	F Panel P2/2	#3&4 Input Bd Pin 31
ECA	Enable Count, CH1 A/D	CH1&2 A/D Pin 23	CH1&2 CTR/Mux, Pin 22
ECB	Enable Count, CH2 A/D	CH1&2 A/D, Pin 35 35	CH1&2 CTR/Mux, Pin 23
ECC	Enable Count, CH3 A/D	CH3&4 A/D Pin 23	CH3&4 CTR/Mux, Pin 22
ECD	Enable Count, CH4 A/D	CH#&4 A/D Pin 35	CH3&4 CTR/Mux, Pin 23
EDT	Edit Mode	F Panel (Button) P3/Y	Out Cont Bd Pin 10
EIP	End Integrate Period (begin count)	Rec Cont Bd Pin 33	#1&2 A/D Bd Pin 26; #3&4 A/D Bd Pin 26
EOD	End of Delay	Trigger & Cont Bd Pin 46	Rec Cont Bd Pin 36
EOO	End of Output	Output Cont Bd Pin 26	Trigger & Cont Bd Pin 51; Output Addr Bd Pin 21; Y DAC & IO Bd Pin 35 (F)

Mnemonic	Description	Origin	Termination
EPT	Ext Plot TB	R Panel 50 Pin Connector Pin 12	Time Base Bd Pin 30
ESB	End of Sweep Blank	X DAC Bd Pin 32	Y DAC Bd Pin 46
ETB	Ext Time Base Command	F Panel (Button) P3/F	Time Base Bd Pin 31
EVA	Enable Vernier Count #1 A/D	CH 1&2 A/D, Pin 24	CH 1&2 Ctr/ Mux, Pin 20
EVB	Enable Vernier Count #2 A/D	CH 1&2 A/D, Pin 40	CH 1&2 Ctr/Mux, Pin 21
EVC	Enable Vernier Count #3 A/D	CH 3&4 A/D Pin 24	CH 3&4 Ctr/Mux, Pin 20
EVD	Enable Vernier Count #4 A/D	CH 3&4 A/D Pin 40	CH 3&4 Ctr/Mux, Pin 21
EXT	Ext Time Base Input	R Panel (BNC) "TB In"	Time Base Bd Pin 28
FLA	Flag (before gating w device Addr)	Out Cont Bd Pin 40	Y DAC Bd 5 (F)
FLG	Flag (gated with Device Addr)	Y DAC Bd 4 (F)	R Panel 50 Pin Conn Pin 18
HDO	Horiz Display Output	X DAC Bd Pin 49	R Panel (through "R" "C" Network in "X-Out" (BNC)
HPN	Horiz. Position Cont	F Panel (Pot) P3/8	X DAC Bd Pin 48
HPO	Horizontal Plot Output	X DAC Bd Pin 47	R Panel (BNC) "X-plot out"
HXB	Horizontal x 2	F Panel P3/16	X DAC Bd Pin 33
HXE	Horizontal x 5	F Panel	X DAC Bd Pin 34
HXJ	Horizontal x 10	F Panel P3/17	X DAC Bd Pin 35
IAA	Input Addr #1	Out Addr Bd Pin 41	Mem Cont Bd Pin 15
IAB	Input Addr #2	Out Addr Bd Pin 45	Mem Cont Bd Pin 19
IAC	Input Addr #3	Out Addr Bd Pin 42	Mem Cont Bd Pin 11

Mnemonic	Description	Origin	Termination
IAD	Input Addr #4	Out Addr Bd Pin 44	Mem Cont Bd Pin 12
ICC	Input Addr Counter Clock	Output Cont Pin 36	Out Addr Bd. Pin 20
ICF	Input Addr counter full	Output Addr Bd Pin 52	Rec Cont Pin 22
JKH	100 µs Time Base (10KHZ)	Time Base Bd Pin 32	Output Cont Bd Pin 48
JMH	10 MHZ Clock	Time Base Bd	Trigger & Cont Bd Pin 18; Rec Cont Bd Pin 37
MAB	Manual Arm Button	F Panel	Trigger & Cont Bd Pin 13
MAB	Manual Arm Button	F Panel P3/1	Trigger Cont Bd Pin 6
MCA	Mem #1 Clock	Mem Cont Bd Pin 43	Mem Bd 2 Pin 31 Mem Bd 1 Pin 33
MCB	Mem #2 Clock	Mem Cont Bd Pin 45	Mem Bd 2 Pin 32 Mem Bd 1 Pin 34
MCC	Mem #3 Clock	Mem Cont Bd Pin 46	Mem Bd Pin 33
MCD	Mem #4 Clock	Mem Cont Bd Pin 44	Mem Bd 2 Pin 34
MCF	Mem Counter Full	Out Addr Bd Pin 27	Out Cont Bd Pin 50
MDG	Mem Data Gate	Not Used at this time	Mem Bd Pin 20
MEA	#1 Mem Addr	Rec Cont Bd Pin 26	Mem Bd 2 Pin 43 Mem Bd 1 Pin 44
MEB	#2 Mem Addr	Rec Cont Bd Pin 13 Output Addr Bd Pin 50	Mem Bd 2 Pin 43 Mem Bd 1 Pin 45
MEC	#3 Mem Addr	Rec Cont Bd Pin 23; Output Addr Bd Pin 51	Mem Bd 2 Pin 44
MED	#4 Mem Addr	Rec Cont Bd Pin 14; Output Addr Bd Pin 53	Mem Bd 2 Pin 45

Mnemonic	Description	Origin	Termination
MIA	Mem Input Bit 1	#1&2 Ctr/Mux Bd Pin 27; #3&4 Ctr Mux Bd Pin 27	Mem Bd Pin 6
MIB	Mem Input, Bit 2	#1&2 Ctr/Mux Bd Pin 28; #3&4 Ctr/Mux Bd Pin 28	Mem Bd Pin 7
MIC	Mem Input Bit 3	#1&2 Ctr/Mux Bd Pin 29; #3&4 Ctr/ Mux Bd Pin 29	Mem Bd Pin 8
MID	Mem Input, Bit #4	#1&2 Ctr/Mux Bd Pin 30; #3&4 Ctr/ Mux Bd Pin 30	Mem Bd Pin 9
MIE	Mem Input, Bit #5	#1&2 Ctr/Mux Bd Pin 31; #3&4 Ctr/ Mux Bd Pin 31	Mem Bd Pin 10
MIF	Mem Input, Bit #6	#1&2 Ctr/Mux Bd Pin 32; #3&4 Ctr/ Mux Bd Pin 32	Mem Bd Pin 11
MIG	Mem Input, Bit #7	#1&2 Ctr/Mux Bd Pin 33; #3&4 Ctr/ Mux Bd Pin 33	Mem Bd Pin 12
MIH	Mem Input, Bit #8	#1&2 Ctr/Mux Bd Pin 34; #3&4 Ctr/ Mux Bd Pin 34	Mem Bd Pin 13
MII	Mem Input, Bit #9	#1&2 Ctr/Mux Bd Pin 35; #3&4 Ctr/ Mux Bd Pin 35	Mem Bd Pin 14
MIJ	Mem Input Bit #10	#1&2 Ctr/Mux Bd Pin 36; #3&4 Ctr/ Mux Bd Pin 36	Mem Bd Pin 15
MLA	Mem #1 Input Latch Clock	Rec Cont Bd Pin 45	Mem Bd 2 Pin 46 Mem Bd 1 Pin 48
MLB	Mem #2 Input Latch Clock	Rec Cont Bd Pin 53	Mem Bd 2 Pin 47 Mem Bd 1 Pin 49
MLC	Mem #3 Input Latch Clock	Rec Cont Bd Pin 46	Mem Bd Pin 48
MLD	Mem #4 Input Latch Clock	Rec Cont Bd Pin 47	Mem Bd Pin 49
MOA	Mem Output, Bit 1	Mem Bd #1&2 Pin 21	X DAC Bd Pin 21; DAC Bd Pin 21

Mnemonic	Description	Origin	Termination
MOB	Mem Output, Bit 2	Mem Bd 1&2 Pin 22	X DAC Bd pin 22; DAC Bd Pin 22
MOC	Mem Output, Bit 3	Mem Bd 1&2 Pin 23	X DAC Bd Pin 23; Y DAC Bd Pin 23
MOD	Mem Output, Bit 4	Mem Bd 1&2 Pin 24	X DAC Bd Pin 24; Y DAC Bd Pin 24
MOE	Mem Output, Bit 5	Mem Bd 1&2 Pin 25	X DAC Bd Pin 25; Y DAC Bd Pin 25
MOF	Mem Output, Bit 6	Mem Bd 1&2 Pin 26	X DAC Bd Pin 26; Y DAC Bd Pin 26
MOG	Mem Output, Bit 7	Mem Bd 1&2 Pin 27	X DAC Bd Pin 27; Y DAC Bd Pin 27
MOH	Mem Output, Bit 8	Mem Bd 1&2 Pin 28	X DAC Bd Pin 28; Y DAC Bd Pin 28
MOI	Mem Output, Bit 9	Mem Bd 1&2 Pin 29	X DAC Bd Pin 29; Y DAC Bd Pin 29
MOJ	Mem Output, Bit 10	Mem Bd 1&2 Pin 30	X DAC Bd Pin 30; Y DAC Bd Pin 30
MTB	Man Trig Button	F Panel P2/L	Trig & Cont Bd Pin 16
MTB	Mon Trig Button	F Panel P2/11	Trig Cont Pin 7
MWA	Mem #1 Write	Mem Cont Bd Pin 23	Mem Bd 2 Pin 35 Mem Bd 1 Pin 40
MWB	Mem #2 Write	Mem Cont Bd Pin 14	Mem Bd 2 Pin 36 Mem Bd 1 Pin 41
MWC	Mem #3 Write	Mem Cont Bd Pin 22	Mem Bd 2 Pin 40
MWD	Mem #4 Write	Mem Cont Bd Pin 17	Mem Bd 2 Pin 41
ODA	Output Data Bit 1	Y DAC Bd Pin 15	R Panel Conn (50 Pin) Pin 24
ODB	Output Data, Bit 2	Y DAC Bd Pin 14	R Panel Conn Pin 25
ODC	Output Data, Bit 3	Y DAC Bd Pin 13	R Panel Conn Pin 26
ODD	Output Data Bit 4	Y DAC Bd Pin 12	R Panel Conn Pin 27
ODE	Output Data Bit 5	Y DAC Bd Pin 11	R Panel Conn Pin 28
ODF	Output Data Bit 6	Y DAC Bd Pin 10	R Panel Conn Pin 29
ODG	Output Data, Bit 7	Y DAC Bd Pin 9	R Panel Conn Pin 30
ODH	Output Data, Bit 8	Y DAC Bd Pin 8	R Panel Conn Pin 31

Mnemonic	Description	Origin	Termination
ODI	Output Data, Bit 9	Y DAC Bd Pin 7	R Panel Conn Pin 32
ODJ	Output Data, Bit 10	Y DAC Bd Pin 6	R Panel Conn Pin 33
ODP	Output Data Polarity	R Panel Conn Pin 23	Y DAC Bd Pin 11 (F)
OMO	Output Mode Off Switch	F Panel P3/19	Output Cont Bd Pin 24; R. P. Conn Pin 19
OPT	Output Present	Out Cont Bd Pin 33	Out Addr Bd Pin 13
PEN	Pen Sig for Plot Output	Out Cont Pin 37	R Panel (BNC) "PEN"
PLT	Plot Output Command	Output Cont Bd Pin 16	Trig & Cont Bd Pin 11; Output Addr Pin 19
POB	Plot Output Push Button	F Panel P3/W	Output Cont Bd Pin 13
POB	Plot Output Push Button	F Panel P3/X	Output Cont Bd Pin 12
POG	Plot Output Enable	Out Cont Bd Pin 29	X DAC Bd Pin 45; Y DAC Bd Pin 41 (F)
POP	Power-on Preset (reset)	Power Supply Pin 35	Trig & Cont Bd, Pin 25; Record Cont Bd, Pin 10; Output Cont Bd, Pin 14; Output Addr Bd, pin 14
PTB	Plot Time Base	Time Base Bd Pin 40	Output Cont Bd Pin 21
PTG	Plot Time Base Gate	R Panel 50 pin, Pin 13	Time Base Bd Pin 37
PTR	Pre-Trig Record Mode	F Panel P2/8	Trig & Cont Pin 17; Rec Cont Pin 25; Output Addr Pin 33
RCA	Reset #1 #k A/D Counter	CH 1&2 A/D Pin 27	CH 1&2 Ctr/Mux, Pin 19
RCB	Reset #2 A/D Counter	CH 1&2 A/D Pin 30	CH 1&2 Ctr/Mux, Pin 45
RCC	Reset #3 A/D Counter	CH 3&4 A/D Pin 27	CH 3&4 Ctr/Mux, Pin 19
RCD	Reset #4 A/D Counter	CH 3&4 A/D Pin 30	CH 3&4 Ctr/Mux, Pin 45
REC	Record Command	Trig & Cont Pin 45	Rec Cont Bd Pin 16; Output Cont Bd Pin 18; Output Addr Bd Pin 11

Mnemonic	Description	Origin	Termination
RIC	Record Interlace Command	Rec Cont Bd Pin 18	Mem Cont Bd Pin 32; Output Cont Bd Pin 19; Y DAC & IO Pin 36 (F)
ROC	Reset Output DAC Counter	Out Addr Bd Pin 12	Out Cont Bd Pin 35; X DAC Bd Pin 10
RPA	R Panel Arm	R Panel BNC "Arm"	Trig & Contr Bd Pin 21
RPA	R Panel Record Status Out	Trig & Cont Pin 50	R Panel 50 Pin Conn Pin 36
RPT	R Panel Trig	R Panel BNC "Trig In"	Trig & Cont Bd Pin 28
RTA	Reset Time Base (one of 2 sep TB Reset Sigs)	Trig & Cont	Time Base Pin 25
RTB	Time Base Reset (Output)	Output Cont Bd 47	Time Base Bd Pin 24
RTO	R Panel Trig Out	Trig & Cont Bd Pin 44	R Panel BNC "Trig Out"
RWE	Remote Write Enable	None (reserved for Boss Para)	Rec Cont Bd Pin 19
SCA	Record Demand Mem Clock	Rec Cont Bd Pin 30	Mem Cont Bd, Pin 35
SCB	Digital Out Demand Mem Clock	Output Cont Bd Pin 49	Mem Cont Bd Pin 33
SEC	Time Base Seconds Command	F Panel (TTL)	Time Base Bd Pin 36
STB	Sample Time Base	Time Base Bd (TTL) Pin 29	Trig & Cont Bd Pin 14; Rec Cont Bd Pin 31
STR	Single Trig Mode	F Panel (button) P3/B	Trig & Cont Bd Pin 19
TAI	Time Base A Interlace	F Panel (TTL) P2/19	Trig & Cont Bd Pin 22; Rec Cont Bd Pin 20
TBG	Time Base B Enable	Trig & Cont Bd Pin 52	F Panel P3/M
TBI	Time Base B Interlace	F Panel (TTL) P2/20	Trig & Cont Bd Pin 32; Rec Cont Bd Pin 24
TBO	Time Base Output	Time Base Bd Pin 28	R Panel (BNC) "T.B. Out"
TBR	Time Base B	Trig & Cont Bd Pin 20	Rec Cont Bd Pin 11

nemonic	Description	Origin	Termination
DB	Time Base ÷ 2	F Panel (TTL) P3/E	Time Base Bd Pin 33
DE	Time Base ÷ 5	F Panel P3/3	Time Base Bd Pin 27
GR	Trig From Comparator	F Panel (TTL)	Trig & Cont Bd Pin 27
MA	Time Base x 10-1	F Panel (TTL) P3/D	Time Base Bd Pin 23
MB	Time Base x 10-2	F Panel (TTL) P3/4	Time Base Bd Pin 39
MH	20 MHz Clock	Time Base Bd Pin 17	# 1&2 A/D Bd Pin 28; # 3&4 A/D Bd Pin 28; # 1&2 Ctr Mux Bd Pin 24; # 3&4 Ctr/Mux Bd Pin 24
PA	Time Base x 10	F Panel P3/C	Time Base Bd Pin 26
RL	Trig Ready Lamp Drive	Trig & Cont Bd Pin 10	F Panel P/22
TO	Time Base x 1	F Panel P3/2	Time Base Bd Pin 35
DO	Vert Display	Y DAC Bd Pin 5/F	R Panel (through R-C Network in Motherboard) (BNC) "Y Out"
PO	Vertical Plot Output	Y DAC Pin 50F	R Panel (BNC) "Plot-Y"
XD	Vert x 4 SW	F Panel P3/T	Y DAC & IO Bd Pin 40
CD	Word Command	R Panel 50 Pin 17	Out Cont Bd Pin 30
RC	Write Command	Rec Cont Bd Pin 27	Trig & Cont Bd Pin 29; Mem Cont Bd Pin 48; Output Addr Bd Pin 22; X DAC Bd Pin 43
RE	Write Enable	Rec Cont Bd Pin 29	Trig & Cont Bd Pin 53
CG	X Ctr Gate	Out Cont Bd Pin 39	X DAC Bd Pin 44; Y DAC Bd Pin 34 (F)
CF	X Counter Full (1023 Cts)	X DAC Board Pin 40	Record Cont Bd Pin 15; Output Cont Bd Pin 31
CK	X Ctr Section Bit 1	Output Cont Pin 25	Output Addr Bd Pin 47; Y DAC Bd Pin 44
CK	X Ctr (Bit 11)	Output Cont Pin 27	Output Addr Pin 24; Y DAC Bd Pin 44 (F)

Mnemonic	Description	Origin	Termination
XCL	XCtr Section Bit 2	Output Cont Bd Pin 28	Out Addr Bd Pin 48; Y DAC Bd Pin 43 (F)
XCL	XCtr (Bit 12)	Output Cont Bd Pin 23	Output Addr Bd P-n 25; Y DAC Bd Pin 47 (F)
XTA	CHA (4096) Output Mode	Out Addr Bd Pin 35	X DAC Bd Pin 19; Y DAC Bd Pin 39 (F)
XTB	CH 5 1&2 (2048) Output Mode (clocked with E00)	Out Addr Bd	X DAC Bd Pin 20; Y DAC Bd Pin 41
XTD	CHS 1-4 vs T Output Command (clocked with E00)	Out Addr Bd Pin 26	Y DAC Bd Pin 47
XYC	CH 2-4 vs 1 output command (clocked with E00)	Out Addr Bd Pin 37	X DAC Bd Pin 15
XYO	CHS 2-4 vs Ch1 Output Switch	F Panel P3/V	Output Addr Bd Pin 30
ZOS	Z output Sig	Y DAC Bd Pin 36	R Panel B.N.C "Z Out"

WARRANTY STATEMENT

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Biomation will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Biomation prepaid and Biomation will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF BIOMATION'S WARRANTY, BIOMATION SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL BIOMATION BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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